THE EDITOR'S VIEW

The Battle for Bragging Rights

Is DEC As Far Ahead As It May Seem?

By Michael Slater

DEC's announcement of its 200-MHz Alpha microprocessor has caused a considerable stir. Can DEC really be this far ahead of the rest of the world? If so, how?—and does it matter?

As I discussed in last issue's editorial, a key reason why DEC can produce faster microprocessors than a company such as Intel or Motorola is its different economic model. DEC knew that if it didn't have astonishing performance, the introduction of a new architecture would create little but stifled yawns. DEC needs Alpha to keep its VMS line competitive, and it can probably justify the entire Alpha development solely on the basis of this product line. No semiconductor maker, however, could justify developing a microprocessor for such a small market. DEC has a number of other advantages as a system maker, such as the ability to provide cooling for a 30-W processor and to tune its semiconductor process to the chip's needs.

HP and IBM, the two other system companies that design and fabricate their own processors, probably aren't far behind DEC. HP has already previewed its next-generation PA-RISC chip, which HP expects to come close to Alpha's performance. Like DEC, HP has focused on achieving high clock rates.

IBM hasn't revealed what it has in store for its future high-end systems, but the mere fact that even its latest high-end systems use a chip set that is three years old is ample evidence that a major new implementation should be close to completion.

MIPS and SPARC are lagging in performance, but this is due in large part to a difference in their business focus: they want to build high-volume systems, not just high-performance systems. The R4000 and SuperSPARC, for example, support a wider range of system configurations than the DEC or the HP processors.

MIPS and SPARC might not, in fact, lag by as much as it seems—at least when it comes to chips that can be used in a mainstream workstation. While DEC promotes its 200 MHz clock rate, the merchant-market chip runs at 150 MHz, and by the time Alpha technology gets to low-cost desktop systems, the clock rate could well be down to 100 MHz (for power dissipation as well as system cost reasons). This is still double Sun's stated target of 50 MHz for SuperSPARC, but Sun's chip has other advantages. While the Alpha chip has a two-cycle load-use penalty, for example, SuperSPARC has none; the branch penalty is also much smaller. SuperSPARC can perform two integer ALU operations in the same cycle, even if one depends on the other, while the Alpha chip can perform only one. SuperSPARC has 36K of set-associative on-chip cache, while Alpha has only 16K of direct-mapped cache, so Alpha's performance will suffer more from cache misses and will be less effective in low-end systems without a second-level cache. Alpha's edge over SuperSPARC for application-level performance will be noticeably smaller than its edge in clock rate.

It is also important to remember that performance is not one-dimensional; simple SPECmark claims obscure the differences between integer and floating-point performance. SuperSPARC will be especially strong in integer performance, for example, because of its ability to issue two integer ALU operations per cycle.

When comparing with R4000 performance, it is important to keep in mind that the R4000 is months ahead of both Alpha and SuperSPARC in its production ramp. By the time its competitors are shipping, MIPS vendors will be sampling versions with higher clock rates and larger on-chip caches, producing a significant performance boost. Its single-issue design will limit floating-point performance, but it will be very competitive for integer applications.

Even so, the R4000 isn't likely to be a performance leader, but that isn't its goal. In terms of SPECmarks per dollar, the R4000—with six competing semiconductor suppliers—is likely to be the leader. DEC, HP, and IBM will probably lead the performance race for the foreseeable future, and this will be critical in high-end markets. In high-*volume* markets, however, it is price/performance at low price points that is most important. This is a key part of Sun's and MIPS' strategy. The importance of low absolute price points is also one factor that could keep either of them from getting much of Intel's market.

All things considered, the performance spread among the various RISCs appears to be caused more by differences in implementation approaches and business focus than by architectural differences or technological advantages. While DEC touts the advantages of the clean Alpha architecture, HP promotes its rich instruction set, and Sun's competitors attack register windows and other possible weaknesses in the SPARC architecture, the differences in implementation style are far more significant than any of these architectural issues.♦