Literature Watch

Buses

Bus-driver ICs. Richard A. Quinnell; EDN, 2/3/92, pg 78, 8 pgs.

Buscon '92 West: Mezzanine buses ride a new wave of popularity. *Less-strict specifications permit mezzanine modules to add functionality without the traditional trade-offs.* Richard Nass; Electronic Design, 2/6/92, pg 35, 6 pgs.

IC-card spec adapts I/O to memory-card slot. *PC-card standard release 2.0 unleashes a myriad of applications.* Richard Nass; Electronic Design, 1/23/92, pg 45, 7 pgs.

Sven Behrendt on: VME's 10th birthday. Sven Behrendt, Force Computers; Computer Design, 2/92, pg 25, 2 pgs.

Development Tools

16-bit-uC evaluation boards: Boards let you try out uC architectures. Ray Weiss; EDN, 2/3/92, pg 41, 8 pgs.

System simulation still holds promise. *Most designers profit from some element of system simulation, but few practice it in pure form.* Lisa Maliniak; Electronic Design, 2/6/92, pg 53, 8 pgs.

Memory

Accelerate DRAM accesses with controller module. *Memory controller trims bus-transfer delays and boosts cache efficiency by manipulating wide memory words.* Dave Bursky; Electronic Design, 2/6/92, pg 47, 3 pgs.

Bidirectional single-bank FIFOs trim system costs. Dave Bursky; Electronic Design, 2/6/92, pg 100, 2 pgs.

Combination DRAM-SRAM removes secondary caches. *Avoid wait states by building simple compact 50-MHz systems with cached DRAMs.* Dave Bursky; Electronic Design, 1/23/92, pg 39, 4 pgs.

Miscellaneous

Electrical-transient immunity: a growing imperative for system design. O. Melville Clark, Donald E. Neill, General Semiconductor Industries; Electronic Design, 1/23/92, pg 83, 6 pgs.

Mobile communications. *WARC-92 must find room in already crowded bands for new worldwide mobile services and expanded existing services.* Edward E. Reinhart; IEEE Spectrum, 2/92, pg 27, 3 pgs.

Profile: Andy Heller against the world. *After 23 fractious years at IBM, the CEO of Hal Computer Systems Inc. doesn't have any regrets—he just wants to get even.* Gary Andrew Poole; UnixWorld, 3/92, pg 34, 4 pgs.

Testability on tap. *Testing loaded digital logic boards becomes much easier with a standard test access port, or TAP, meant for boundary-scan tests.* Colin M. Maunder, BT Laboratories; and Rodham E. Tulloss, AT&T Bell Laboratories; IEEE Spectrum, 2/92, pg 34, 4 pgs.

What are multichip modules, and why should you care? *A new form of hybrid IC will be an $18 billion market by the year 2000, as 30% of all chips will be sold as part of a module.* Hugh G. Willett; Electronic Business, 1/27/92, pg 48, 3 pgs.

Peripheral Chips

Control systems and audio drive DAC resolution. Jeffrey Child; Computer Design, 2/92, pg 111, 4 pgs.

Try single-slope A-D conversion for a low-cost 12-bit solution. *Microcontroller-based design uses minimal support ICs and code to get high-accuracy analog-to-digital conversion.* Kevin Daugherty, National Semiconductor Corp.; Electronic Design, 1/23/92, pg 59, 6 pgs.

VGA chip ups colors, speeds graphics with local bus interface. Dave Bursky; Electronic Design, 2/6/92, pg 103, 1 pg.

Processors

DEC's big gamble on a new RISC. *A 200-MHz CPU is the first in a family that will power everything from palmtops to supercomputers.* Lawrence Curran; Electronics, 2/92, pg 38, 2 pgs.

Microcontrollers span 8- and 16-bit applications. Dave Bursky; Electronic Design, 1/23/92, pg 139, 2 pgs.

RISC is simple but benchmarking isn't. *Measuring the performance of RISC-based designs is a lot like benchmarking traditional processors—only worse.* Tom Williams; Computer Design, 2/92, pg 67, 6 pgs.

Real-time DSPs target multimedia motherboards. Dave Wilson; Computer Design, 2/92, pg 36, 2 pgs.

Programmable Logic

EPLD combines 80-MHz counter rate with 256 logic cells and 164 I/Os. Ray Weiss; EDN, 2/3/92, pg 75, 2 pgs.

Enhanced EPLDs tackle 70-MHz systems. *High-density UV-EPROM-based programmable logic devices also deliver top I/O.* Dave Bursky; Electronic Design, 1/23/92, pg 135, 3 pgs.

One-upmanship in competitive FPGA contest. Barbara Tuck Egan; Computer Design, 2/92, pg 30, 2 pgs.

Programmable interconnection matrix in silicon speeds system design. Dave Bursky; Electronic Design, 1/23/92, pg 31, 2 pgs.

System Design

Multiprocessing to bring the next jump in performance. Warren Andrews; Computer Design, 2/92, pg 78, 11 pgs.