Most Significant Bits

IDT and Toshiba to Collaborate on MIPS Chips

Integrated Device Technology and Toshiba have announced an agreement to collaborate on the development of MIPS derivatives and to alternate-source each other's designs. Siemens previously entered into similar agreements with both IDT and Toshiba, so at least some of the MIPS derivative processors will have three sources. In addition to providing alternate sourcing, the companies will share development resources and cell libraries.

With the exception of the IDT/Siemens agreement for Siemens to alternate-source IDT's R3051, MIPS derivatives designed by the semiconductor partners have been sole-sourced. From the semiconductor vendor's view, this can be an advantage, since it gets them out of the six-way pricing war they must endure for the standard MIPS designs. It has resulted in considerable redundancy of effort, however, as several of the MIPS partners have independently embarked on similar, but slightly different, derivatives. With the emergence of the R4000 as a new base processor, the task of developing derivatives has become even more complex.

Toshiba brings to the party its strength as an ASIC vendor, and it will offer its customers the ability to combine IDT's R3051 and R3081 cores with peripherals and other functions from its cell library. Toshiba will also market the standard R3051 and R3081 products, as well as the R3500 (a combination IU/FPU without on-chip cache). Siemens also has the option to alternate-source the R3081 but has not yet done so.

IDT and Toshiba plan to codevelop new MIPS derivatives for the embedded and general-purpose markets. The first new derivative will be a lower-cost version of the R3051. Following this device will be versions with additional on-chip peripherals for applications such as telecommunications and networking. Next year, several R4000 derivatives will be introduced, including a 75-MHz version for higher-performance, and cost-reduced versions for low-end ACE/ARC systems.

LSI Logic Launches CoreWare Program

In an effort to broaden the application of its processor cores, primarily in embedded applications, LSI Logic has launched its "CoreWare" program to offer customers the ability to combine processor cores with other megacells and customer-designed circuits. CoreWare products are distinguished from conventional ASICs primarily in the amount of design support LSI will provide, which will include test vectors, behavioral models, and simulation tools. LSI will also be more involved in system architecture and partitioning than it is in a typical ASIC design. LSI has formed a new division, led by Moshe Gavrielov, that is dedicated to the CoreWare program.

Microprocessor cores available include:

- The LR33000 embedded MIPS processor, which can be used with or without caches, peripherals, and bus interface logic.
- A SPARC core, which is a basic SPARC integer unit
- A 1750A core for military applications.

IEEE-compatible floating-point cores include pipelined and non-pipelined 32-bit ALUs and multipliers; a pipelined 32-bit divider; and non-pipelined 64-bit ALUs and multipliers. Peripherals include a SCSI controller, an SBus DMA controller, and a multiprocessor bus interface. Other cores due later this year include a JPEG compression engine, a Reed-Solomon error correction unit, and a MIPS processor with a floating-point unit.

Use of the CoreWare cores requires payment of a one-time license fee, which ranges from $25,000 to $80,000 per core, plus a per-unit royalty. The cores are initially implemented in a 1-micron technology, but they will be moved to a 0.6-micron process in the second half of this year. With the 0.6-micron technology, it will become practical to add considerable custom logic to the LR33000 processor core.

Until now, high-performance CPU cores have not been generally available as ASIC cores. The leader in this area has been VLSI Technology with its ARM core, but this processor does not match the performance of the MIPS and SPARC designs and does not have comparable software support. NEC has offered its V-series processors as ASIC cores, but these are not in the same performance league. LSI's closest competitor in the future may be Toshiba, as a result of the IDT/Toshiba agreement that gives Toshiba access to the R3051 and R3081 cores.

The availability of high-performance processors as ASIC megacells is an important trend, since the level of integration has reached a point where it can be economical to combine the processor core with the peripherals and interface logic that are traditionally implemented with standard chips. As more functions are combined on one chip, however, the device becomes more application-specific. Vendors of standard processors are hesitant to narrow the market, so they tend to leave off functions that aren't applicable to a broad range of applications. The ability to use standard, high-performance processor cores in ASICs will let system designers tailor the on-chip functions to their needs.

IIT Introduces Data Compression Chip

Integrated Information Technology has announced its first loss-less data compression chip, the IIT-DCP. IIT is

best known for its Intel-compatible math coprocessors, and it has more recently entered the video compression processor business.

The IIT-DCP is designed for use on a PC system board and in dedicated computer systems to provide automatic compression of files as they are written to disk and decompression as they are read from the disk. Image compression algorithms can achieve compression ratios of 25:1 and higher, typically using the JPEG algorithm, but they discard data that is not noticeable in the image. Data compression algorithms, on the other hand, are most commonly based on variations of the Lempel-Ziv (LZ) algorithm and achieve only 2:1 compression on average, but they preserve every data bit. Thus, they can be used on all data and program files.

Automatic data compression is likely to become a standard feature in portable systems, where hard disk capacities are limited by physical size constraints. Software implementations are already popular for this application. Data compression is also useful in desktop systems, where it often represents the least expensive way to increase disk capacity and speeds network data transmission.

Competitive chips are already available from InfoChip, Stac Microelectronics, and AHA. IIT claims that its chip is considerably faster than all of its competitors and is also the only single-chip implementation. The competitive devices require external SRAMs for the dictionary, and they perform an iterative search that typically requires several clock cycles for each byte that is compressed.

The IIT device, on the other hand, stores its dictionary in an on-chip content-addressable memory, performing an exhaustive look-up in a single clock cycle. IIT claims that this approach is not only faster but also provides about 20% better compression because the search is more complete. With a 33-MHz clock, IIT claims a sustained compression/decompression rate of 5 Mbytes/s, while the closest competitor (in terms of performance)—Stac's device—is capable of only 2 Mbytes/s peak and less than 1 Mbyte/s sustained.

The IIT-DCP interfaces directly to a 16-bit ISA (AT) bus, and it can also be easily interfaced to the processor's local bus. The chip is implemented in 1-micron CMOS and is 320 mils square. Packaged in an 84-pin PLCC, it is priced at $30 in quantities of 10,000. IIT has fabricated first silicon and expects second-pass chips correcting a few minor bugs in late March. Production is planned for the second quarter.

Echelon Adds Modules, DOS API

Now that the Echelon NEURON chips are in production and are available from Toshiba and Motorola, Echelon has introduced its first module-level products. These are the first products, other than development systems, to be sold directly by Echelon.

The modules combine a NEURON chip with a clock generator and a twisted-pair transceiver, relieving the system designer of the task of implementing the transceiver function. The lowest-cost module, priced at $35 in volume, uses an RS-485 interface and operates at up to 78 kbps. A transformer-isolated module using Manchester coding at the same data rate is available for electrically noisy environments. For applications requiring high data rates, a version of this module is available with a 1.25 Mbps data rate.

Echelon also introduced a set of C-language software libraries for DOS-based computers, called the LONMANAGER API for DOS, to simplify the creation of PC-based controllers for network installation, management, and control. The libraries are priced at $9850, plus a royalty of $120 to $190 per system into which they are incorporated.

Motorola to Supply SBus Interface Chips

Sun and Motorola have announced two new SBus support chips that were designed by Sun and will be available on the open market from Motorola. This is indicative of a shift in Sun's ASIC suppliers, since previous devices have come from LSI Logic. Rumors are that the relationship between LSI and Sun has become quite strained.

The "SBus Goldchip" is a DMA controller that operates as an SBus master. Unlike the current SBus DMA chip available from LSI, the Goldchip implements the 64-bit transfer protocol of the Revision B.0 SBus specification, using the address lines in addition to the data lines to provide the 64-bit path. Sun claims a sustained bandwidth of 160 Mbytes/s.

The second chip is the "SBus SLIC," a general-purpose, 32-bit SBus slave interface designed for cost-sensitive I/O boards that do not need DMA. Peak bandwidth is claimed to be 80 Mbytes/s, but the actual bandwidth will be limited by the speed of the system.

Availability of both chips is planned for the fourth quarter of 1992. Pricing has not been released.

Errata

In the table on page 15 of our 1/22/92 issue, some of the information for LSI's MIPS processors is incorrect. The LR33000 is available in a 160-in MQFP at all clock rates. Pricing for the 25-MHz version is $89, and the 40-MHz version is $145. For the LR33020, the packages are a 224-pin PGA or a 208-pin MQFP, and the chip is available in 25-, 33-, and 40-MHz speeds. The 40-MHz version is priced at $217 and consumes 600 mA.

On page 9 of our 2/12/92 issue, we refer to the future R4000 version with a "75 MHz (100 MHz internal)" clock rate. This should have said 75 MHz (*150* MHz internal)."♦