Intel's 386 Patents Appear to be Avoidable

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Here are brief descriptions of the five patents Intel claims the C&T Super386 violates. It appears that most of these patents are not fundamental to 386 compatibility; workarounds are quite clear in some cases. Prior art is likely to exist for at least some of the patents. Intel disagrees, of course, and claims that the '338 and '944 patents are inherently infringed by any processor that is 386-compatible.

Disclaimer: The author is neither an attorney nor a patent agent. Do not construe anything in this article to be legal advice. The remarks set forth below are merely the author's opinions from an engineering point of view.

Patent 4,363,091, filed 1/31/78, issued 12/7/82: "Extended address, single and multiple bit microprocessor." Claim 1 describes the way the 8086 and 8088 generate physical addresses by shifting the segment base left by four bits and adding it to the offset, "to result in an address word greater in bit length than the maximum bit length stored in said plurality of registers, whereby said data processing system is afforded an extended memory space beyond the address word length limitation of said plurality of registers."

An alternative implementation could perform the shift before storing the segment base, and, of course, store it in registers four bits wider than the 8086 used. Such an implementation would differ from the '091 patent in that there is no shift operation, the address word is equal to and not "greater in bit length than the maximum bit length stored in said plurality of registers," and the memory space does not extend "beyond the address word length limitation of said plurality of registers." Claims 2 through 23 depend on claim 1, and claim 24 is very similar.

Claim 25 allows 16-bit operations on 8-bit immediate data by extending the sign bit of the data byte into the upper 8 bits, when a certain bit in the opcode is zero. While I have not yet taken a look, surely C&T can easily find prior art for sign extension under opcode control. The last claim, 26, is a method corresponding to the apparatus of claim 25.

Patent 4,447,878, filed 8/10/81, issued 5/8/84: "Apparatus and method for providing byte and word compatible information transfers." The circuit of claim 1 can transfer an odd byte bidirectionally to, and from, the low-order byte of the bus. Claim 6 is similar, renaming first and second buses to be local and system buses, and claim 8 specifies the decoding of some command signals. The rest of the claims each depend on one of these three independent claims.

Patent 4,449,184, filed 11/18/81, issued 5/15/84: "Extended address, single and multiple bit microprocessor." This patent is based on the 8086/88. "We claim: 1. ... instructions obtained from said memory are temporarily stored in said queue until requested... for execution." Yikes! The instruction queue patent! C&T might be able to find prior art in just about any corner of the computer universe. An alternative would be to create a small instruction cache that includes some prefetching. This would improve the performance of the microprocessor, and it would not contain the stated "plurality of registers forming an ordered, first-in-first-out queue of registers," since branches would cause the cache to provide its data out-of-sequence. All other claims depend on claim 1.

Patent 4,972,338, filed 4/19/88 (continuation of a 6/13/85 application), issued 11/20/90: "Memory management for microprocessor system." Claim 1 describes the 386 memory management and protection mechanism, including comparing the virtual address against the segment descriptor limit, adding the virtual address to the segment base (these first two steps being done by the segmentation unit), comparing the resulting linear address page field against the page cache tags and if none match, going out to main memory for the missed page table entry, and finally connecting either to (i) the linear address or (ii) combining the linear address offset with the page entry, to form the physical address.

Another way to achieve this function involves the last step, termed the address generating means. It produces the physical address either from (i) the linear address from *said* segmentation unit, or from (ii) the offset combined with the page entry. Add a new element, perhaps called an auxiliary unit, which, like the segmentation unit, adds the segment base to the virtual address, and connect the address generating means to the auxiliary unit instead of the segmentation unit. This results in a compatible implementation that differs substantially in its structure.

Patent 5,053,944, filed 10/3/90 (continuation of a 11/15/88 application) issued 10/1/91: "Microprocessor breakpoint apparatus." This invention compares a variable-width breakpoint address with the virtual address of an instruction fetch or data reference

and generates a breakpoint signal if a bit is set in a control register. Notice that this circuit does more than a software patch, since it can break on data accesses as well as instruction fetches.

An alternative circuit would, rather than having one comparator determine if there is an exact match, have two comparators checking to see if the virtual address is greater than one limit and less than another, and, if so, generating a breakpoint signal. The bounds for the two comparators would be computed at the time the breakpoint address is loaded, as follows: the greater-than comparator would be fed the breakpoint address minus one, and the less-than comparator would be fed a value depending on the width of the breakpoint address. If the breakpoint address is to an individual byte address, this register would be set to the address plus one. If it is to a word, it would be set to the address plus two, and if to a double word, the address plus four.

Thus, we have achieved compatibility with the 386, but in addition, we have the components in place to set a breakpoint to occur for any access within a range of addresses, rather than for a single address. Also, the comparator described in the patent is used 'to determine a match between two addresses,' while one of the comparators in the workaround solution is to determine if one address is less than the other, and the second comparator determines if one address is greater than another. Since this circuit apparently does not contain at least one of the elements in '944, it would differ substantially.

Other Patents

Among Intel's collection of over 360 U.S. patents, there are several others that appear to relate to the 386 microprocessor. It is not clear why Intel did not assert these patents against C&T. Examples of such patents include:

Patent 4,270,167, filed 6/30/68, issued 5/26/81: "Apparatus and method for cooperative and concurrent coprocessing of digital information." Pertains to the way the 386 and 387 share the local bus and the system bus.

Patent 4,442,484, filed 10/14/80, issued 3/10/84: "Microprocessor memory management and protection mechanism." Describes how the 286, and so the 386, does protected-mode addressing using descriptor tables in memory.

Patent 4,860,195, filed 11/15/88 (continuation of an application filed 2/24/86), issued 8/2/89: "Microprocessor Breakpoint Apparatus." This patent is very similar to patent 5,053,944, which is one of the ones Intel *did* assert against C&T. In fact, '944 is a continuation of an application which itself was a continuation of this patent. ♦

Intel Sues C&T

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C&T's detailed internal chip design can determine whether C&T does, in fact, violate these patents, it appears to be possible to work around them. Intel claims, however, that two of the patents—'338, covering the memory management scheme, and '944, covering the breakpoint mechanism—are infringed by any processor that is 386-compatible.

C&T claims to have studied Intel's patents extensively before designing its chips, and it asserts that it does not violate the patents. C&T CEO Gordon Campbell claimed that "Intel's lawsuit is a continuation of its policy to exert a monopoly over the microcomputer industry.... Its latest tactic is to file this legal action in an attempt to delay the adoption of our superior microprocessors by the computer industry."

Conclusions

It is impossible for us to judge, at this point, whether or not C&T's chips do indeed infringe Intel's patents or whether the patents could be invalidated if challenged. For the near term, however, these issues aren't even relevant; the mere act of filing this lawsuit will make it difficult for C&T to get design wins for its microprocessors. C&T may be able to get some customers to use its 38600 devices, which are pin-compatible with Intel's, but the cloud of uncertainty that Intel's legal action puts on the chips is likely to dissuade any major companies from designing systems around C&T's enhanced 38605 chips, which have additional signals and therefore require special support in the system design.

At the recent CeBIT show in Germany, C&T claims that 27 companies announced computers using C&T's Super386 processors. Nearly all of these companies are Taiwanese, however, and none are recognized names, at least in the U.S. market.

The foundry license issue is a critical one for C&T, as it is for Cyrix and USLI. If Intel loses the ULSI appeal, it could set a precedent that would greatly strengthen C&T's defense. If this occurs, an out-of-court settlement seems likely.

The lawsuit comes at an especially difficult time for C&T, which has lost considerable parts of the chip-set business to competitors and has suffered from decreased margins on the chip-set business that it has kept. The new microprocessors and coprocessors are the key to C&T's future, and Intel has placed this future in jeopardy. It is most fortunate for C&T that TI has intervened, since this gives C&T much more legal muscle—and possibly some financial backing—for fighting Intel.♦