Nimbus Unveils MBus Chip Set

Startup's Chip Set Offers MBus Graphics

By Brian Case and Michael Slater

Despite the grand predictions of Sun Microsystems, the SPARC-based, Sun-compatible workstation market has remained small since Sun shocked the computer world with its intention to make SPARC an open standard. Now, with the announcement of its MBus-based, NIM6000M board kit, tiny Nimbus technology of Santa Clara would like to help make the SPARC-compatible workstation market grow.

Nimbus is a 10-person company that was formed by former Via Technologies engineers, led by Nimbus president Sanjeev Renjen, when Via decided to abandon its SPARC chip set project. Seed capital came from the founders; Cypress Semiconductor funded the product development but has not made an equity investment. Nimbus is allowed to sell this chip set only with a PC board as a complete kit; Cypress has the exclusive rights to market the chips alone. An equity investment is expected to be announced soon by a Far East partner.

Nimbus' first product was the NIM6018 SBus DMA controller, announced in February of this year, which is pin-compatible with LSI Logic's SBus DMA chip. This chip is most commonly used to interface an Ethernet and SCSI controller to the SBus, Sun's I/O bus. In addition to the SBus DMA chip, the new Nimbus chip set has five other chips: a memory controller, a peripheral I/O controller, a timer/interrupt controller, a graphics controller, and an MBus-to-SBus interface.

The Chip Set

Rather than striving for minimum chip count, Nimbus decided to use a larger number of chips to keep die size and package cost to a minimum. As shown in Figure 1, the memory controller chip (NIM 6033) is actually a 32-bit slice due to pin limitations on inexpensive packages. Therefore, a full chip set requires two memory controllers (for a total of seven chips) to implement a 64-bit MBus memory interface. The memory controller supports DRAM configurations from 8 MB to 128 MB in steps of 8 MB using a variety of standard DRAM SIMMs (1M × 9, 4M × 9, 1M × 36, or 4M × 36). Space constraints limit the NIM6000M board to 96 MB of memory. To allow MBus writes to complete quickly, the memory controller implements a four-deep write buffer.

The peripheral I/O controller (NIM6024) converts MBus cycles into 386SX-protocol cycles. For most systems, the 6024 will be used solely for its glueless interface to up to eight on-board devices. The 386SX-compatible bus also allows an AT bus interface to be added, if desired, using a standard PC system-logic chip. Seven standard devices are implemented on the 6000M board: a boot EPROM, two serial ports, keyboard and mouse interfaces, a floppy disk controller, a real-time-clock/non-volatile RAM chip, an ISDN/Audio interface, and the NIM6005 interrupt controller.

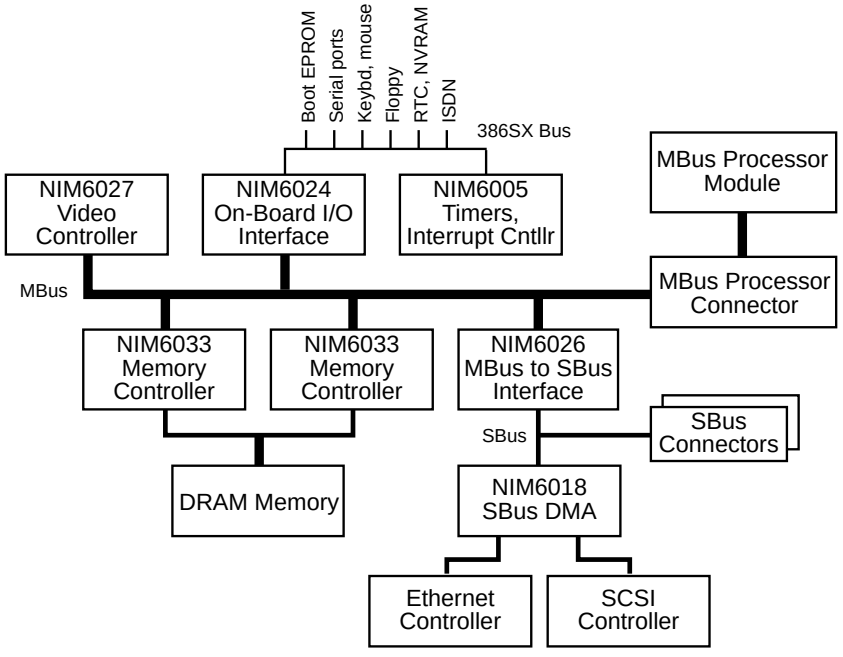

Figure 1. Block diagram of the Nimbus system.

The 6005 chip implements two 32-bit counters and the logic for the standard SPARC 15-input interrupt prioritization and masking. The counters are clocked by a dedicated time-base input. One use for the counters is to generate interrupts for system profiling. The 6005 provides both active-high and active-low interrupt inputs, supporting any mix of SBus-style (active low) and PC/AT-style (active high) interrupt signals.

The graphics controller (NIM6027) is software-compatible with Sun's 1152 × 900 color and monochrome display standards. Though the 6027 has no special graphics acceleration hardware, it achieves high

Price & Availability

The Nimbus chip set with a blank PC board (but none of the other components for the board) will sell for $350 to $400 in quantities of 1000. Samples are available now, with production in August.

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performance for graphics operations by being a resident on the 40-MHz, 64-bit MBus. Compared to the 20-MHz, 32-bit, SBus-resident Sun display controllers, the 6027 benefits from the extra width and higher speed of MBus. Nimbus claims that the 6027 performs comparably to Sun's accelerated GX graphics controller, at a much lower cost, for commercial applications. For applications involving 2-D or 3-D rendering, the GX is faster. One benefit of the Nimbus approach is that graphics performance will scale with CPU performance, unlike a system with a separate graphics engine.

The MBus to SBus interface chip (NIM6026) translates MBus transactions to SBus transactions and vice versa; it allows master and slave transactions from both sides. The 6026 supports three SBus slots. The chip also has an eight-entry TLB for translating virtual SBus addresses into physical MBus addresses.

Competition

LSI Logic announced an MBus chip set over two years ago (see µPR 4/4/90, p. 1), and Fujitsu announced one last year (see µPR 5/29/91, p. 1), but both of these products have encountered numerous delays and have only recently become production-ready; LSI has not yet shipped a 40-MHz chip set. Both the Fujitsu and LSI chip sets offer lower chip count, since they implement the DRAM controller in a single device. Fujitsu's chip set goes the furthest, combining the DRAM and I/O control functions as well as a display controller on a single chip. Nimbus believes that it can be cost-competitive, despite the higher chip count, because of the lower-cost packages.

Both Nimbus and Fujitsu provide a graphics controller interfaced to the MBus, giving them higher display bandwidth than systems using SBus graphics cards. One drawback of this approach is that it requires that the graphics be part of the system board, so it does not allow system makers to offer a variety of graphics options. Of course, the on-board graphics can always be ignored if the system customer wants to upgrade the system with an accelerated graphics card plugged into the SBus.

LSI and Fujitsu have generally bundled their chip sets with their microprocessors. Not being in the processor business, Nimbus does not have this option—but with the emergence of SuperSPARC and hyperSPARC, neither the LSI nor the Fujitsu processors will be the preferred solution for long.

Sun's only MBus-based workstation is the new SPARCstation 10, which starts at $18,495 (see p. 11). The Nimbus chip set (or the LSI or Fujitsu chip set) will allow compatible system makers to build competitive systems at lower prices—once the SuperSPARC or hyperSPARC processors become available to them. Nimbus will have to compete with Sun's own SS-10 chip set, marketed by LSI Logic (see box). The Nimbus chip set will be available sooner, however, and it is likely to be significantly less expensive because of the lack of Sun royalties.

Comparisons to Tera Microsystems are inevitable, since Nimbus and Tera were both founded to make chip sets for SPARC-based systems. Tera was closed down earlier this year when its backers declined to continue funding, and Tera founder Henri Uehara has cited the small size of the Sun-compatible market as the reason for the company's inability to get continued funding. One key factor limiting the Sun-compatible system market is the lack of an effective distribution channel; few, if any, of the compatible system makers are in a position to deploy a sales force close to the size and experience of Sun's, and Sun has blocked access to the next obvious channel—the value-added resellers. Sun's aggressive system pricing, sales force, and business practices make it a tough umbrella to live under.

Nimbus could face the same problems as Tera, but it is much better positioned in several respects. First, Nimbus has the entire chip set working, while Tera

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SS10 Chip Set from LSI Logic

Concurrently with the SPARCstation 10 announcement, LSI Logic announced that it will offer on the merchant market the five ASICs in Sun's new system. This is the first time that Sun has not delayed licensing of the ASICs until months after systems were shipping. Samples are promised for the third quarter, with volume production "shortly thereafter." Sun still maintains quite a lead over prospective clone makers, since it would be year-end, at best, before anyone else could be in a position to ship systems based on the chip set. No pricing has been released.

The five-chip set consists of the L64860 Enhanced Memory Controller (EMC), the L64861 32-bit to 8-bit controller (SEC), the L64862 MBus-to-SBus interface (MSI), the L64854 SBus DMA controller (DMA2), and the L64863 clock generator (CLK2).

onics. Fault tolerance and high availability have a very high priority for this application. The ability to develop solutions using commercial grade hardware and then to convert those solutions into mil-spec hardware is very important in this application.

The telecommunications application is differentiated by its strict requirements for high availability, fault tolerance, and maintainability for systems that operate continuously. Live insertion will probably be used to help meet these requirements. Maintaining consistency with the world-wide telecommunications equipment standards (ETSI and NEBS) is also a high priority.

Current Status

Several manufacturers are now offering the full gamut of hard metric mechanical pieces that board and systems builders require. Included in this list are enclosures, backplanes, connectors, prototype boards with transceivers, and test fixtures.

BTL transceivers are available from several manufacturers, including National Semiconductor, Signetics, and Texas Instruments, in configurations ranging from 4-bit to 9-bit parts. These same companies plus Newbridge Microsystems are either shipping or have announced protocol controllers for several of the application areas.

A small number of processor, memory, and I/O boards have just become available from several companies. Boards from different vendors have been demonstrated working together in a single backplane. Systems companies have shown working systems with all internally designed boards, and with a mix of internally and externally designed boards.

Data acquisition boards for two of the top selling logic analyzers have been demonstrated. Each of the respective boards interfaces between the logic analyzer's probes and the bus, while maintaining the required Futurebus+ electrical environment. Both analyzers can display either timing or state information with transaction information decoded and presented as text.

Conclusions

Futurebus+ has arrived. Sufficient investment has been made to insure its success in several different markets. A solid technical foundation has been laid that combines newly invented technologies with some of the best of previously proven technologies. This foundation will support several generations of designs across an increasingly wide range of applications. While far from perfect in terms of both its design and its implementation, this time around Futurebus+ is "good enough."♦

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never completed its SBus interface chip. Second, Tera did not use the MBus, and was thus cut off from the emerging generation of processors. Finally, Tera built a relatively large organization with high cash requirements, while Nimbus has a fraction of Tera's overhead.

Market Potential

Nimbus plans to sell only the board kit, which consists of the seven Nimbus ASICs and a PC board that fits into the standard SPARCstation pizza-box enclosure, making system design as easy as possible for Nimbus' customers. A port of SunOS to the Nimbus system design is nearing beta release from Interactive Systems. In a striking departure from previous MBus chip set announcements, Nimbus already has a working version running OpenWindows on their hardware.

Nimbus claims its system will perform about 15% better than a SPARCstation-2 because cache misses are handled in 17 processor cycles, instead of 26 processor cycles for the SS-2. This is due, in large part, to the fact that the SS-2 does not use the MBus, and the DRAM is interfaced to the slower SBus. The performance claim assumes a cache miss rate of 2.5%, so the actual performance difference will depend on the application.

Since the Nimbus chip set implements the MBus level-2 protocol, system performance can be increased with dual-processor MBus modules. Capacitive loading problems prevent use of more than one MBus connector with the current chip set. Nimbus is planning a second generation that will handle more than one MBus module and operate much faster (between 50 and 60 MHz).

At long last, it appears that a variety of MBus SPARC processors will be available (see p. 1). This will give clone makers using the Nimbus chip set a simple way to differentiate their systems in the marketplace and yet offer easy upgradeability. Nimbus says the level of interest in MBus has increased dramatically because the SuperSPARC and hyperSPARC announcements make it clear to system makers that MBus and SPARC are finally "real." System makers can use the existing Cypress/Ross MBus module, based on the older 7C601 processor, and upgrade to SuperSPARC or hyperSPARC when those products become available.

Nimbus' chip set and board seem to be a simple, high-performance way for system makers to test the SPARC-clone waters. If the interest is really there among system makers and if the market is really ready to buy SPARCstation clones in large numbers, Nimbus is in an excellent position to reap some profit and set the direction for the next generation of SPARC-based computers. ♦