Most Significant Bits

First Silicon on Intel's P5

According to unofficial sources, Intel's P5 (586) was taped out the week of April 20, and testing of the first silicon began about two weeks ago. It is fabricated in BiCMOS—Intel's first processor using this technology. The chip incorporates about 3.5 million transistors and is nearly 640 mils (16.2 mm) on a side, making it even bigger than TI's SuperSPARC (which is also fabricated in BiCMOS). The target clock rate is 66.7 MHz.

The formal announcement is planned for the fall. A slew of system announcements is likely by fall Comdex, but volume shipments are unlikely before early '93. A chip of this complexity will probably take some time to get fully debugged and into production, despite a mammoth effort by Intel to make the initial silicon as clean as possible. In addition to the usual simulations, a hardware emulation using an array of Quickturn's FPGA-based ASIC emulators has been used to verify the design. The BiCMOS process adds an additional factor of risk to the schedule, since the process will be somewhat unproven in addition to the chip design itself.

Texas Instruments Announces 486SLC Plans . . .

As expected, Texas Instruments announced that it will begin marketing the Cyrix-designed 486SLC under its own name, in addition to fabricating the chip for Cyrix. TI plans to be in production in September; no pricing has been announced. Intel does not have any clear point of legal attack against TI, since TI has a patent cross-license agreement with Intel that covers all Intel patents applied for through 1985. TI's legal protection is not so clear for future products, however, which may infringe Intel's newer patents.

In addition to marketing the 486SLC, TI has rights to market future designs from Cyrix, and it plans to develop highly integrated processor/system logic chips using the Cyrix core.

. . . and Intel Slashes Prices on 486SX

Intel's attempt to replace the 386DX with the 486SX has begun in earnest. The company recently announced its third-quarter pricing for the 486SX: $99 for 16- and 20-MHz versions, and $119 for the 25-MHz model (in thousands). These prices are as much as 58% less than the second-quarter prices, which are $144 for 16 MHz, $201 for 20 MHz, and $282 for 25 MHz. (All prices are for PQFP.) This will bring the 486SX down to the current pricing for the 386DX. As a result, 386DX prices will have to drop sharply as well, but Intel has not announced third-quarter prices except for the 486SX.

Intel attributes the dramatic price cut to the new revision of the silicon, which actually eliminates the FPU from the die instead of simply disabling it. The reduction in die size is a mere 12%, however: in the 0.8-micron process, the die size drops from 127K mils^2 to 112K mils^2, while the 1-micron version drops from 270K mils^2 to 240 mils^2. (Intel is building the chip in both processes to maximize production capacity.)

The driving force for the price cut is clear: it is an attack on AMD's 386 sales and a pre-emptive strike against Cyrix's (and now TI's) 486SLC and AMD's future 486SX. The price cut will force Intel's competitors to cut their prices, reducing their profit margins and thereby cutting their bankrolls for their attack on Intel's market share. (Cyrix's 486SLC has been priced at $119 in thousands—a price that must drop significantly in response to Intel's action.)

By the end of this year, the 486SX should be near $80, with the 386DX below $70 and the 386SX under $40 (all for low clock rates, with the top clock speeds commanding a modest premium). At these prices, the 386 and 486SX market will still be profitable, but it will no longer be the gold mine it once was—for Intel or its competitors. The 486DX is still at a relatively stratospheric $406 to $570, depending on clock rate, but this price is likely to plummet—perhaps to the $200 range—by the end of the year, as AMD moves its 486 into production and Intel begins shipping the P5.

NexGen Seeking New Funding

NexGen Microsystems is seeking to raise $15 to $30 million in a private placement offering. According to sources familiar with the private placement memorandum, issued by sales agent PaineWebber, NexGen anticipates that the minimum $15 million it is seeking to raise will carry them through early 1993, and the maximum $30 million would carry it through the end of '93. The company has apparently exhausted its initial capital and is operating on $1.75 million in bridge loans from Kleiner Perkins, ASCII Corp., and Olivetti.

NexGen expects to ship systems based on its chip set, priced from $7,000 to $15,000, in the second half of this year. A prototype system has been successfully tested for compatibility by an independent testing lab, VeriTest, including running Windows 3.0 in protected mode and a variety of DOS applications. Curiously, the tests were made without a mouse or a floppy disk drive, suggesting that some problems were avoided. No UNIX software was tested, the system tested did not include an FPU, and branch prediction was disabled. VeriTest did not find any compatibility problems. It did not measure performance.

NexGen plans to reduce its initial eight-chip implementation, currently being fabricated by Yamaha, to a

three-chip design using 0.5-micron CMOS from another foundry. While the company will initially focus on selling complete systems based on the 8-chip set, it intends to sell the 3-chip set to other system makers.

Beating Intel's performance is key to NexGen's viability, and this won't be easy. The company expects the initial eight-chip set to run at 33 MHz and perform at 25 SPECmarks, about twice the performance of a 486 at that clock rate. The three-chip version is expected to run at 66 MHz and deliver 60 SPECmarks (1989). These performance levels may enable NexGen to compete with 486 systems, but the 33-MHz version will be much slower than Intel's P5, which won't be far behind in its production schedule. The three-chip, 66-MHz version promises to be more impressive, but it is not clear that it will outpace the P5.

Intel Announces 960CA Upgrade

Intel has announced the 960CF, an upgraded version of the 960CA. The new device quadruples the instruction cache from 1K to 4K bytes and adds a 1K-byte data cache (the 960CA has data RAM but no data cache). The data cache is direct-mapped and write-through. The instruction cache, like that in the 960CA, is two-way set-associative. The 960CF is code- and pin-compatible with the 960CA, and it is based on the same CPU core.

According to Intel's benchmarks, the larger instruction cache and new data cache boost performance by 37% to 95% on PostScript performance tests, using a QMS 1700 printer with DRAM memory. On Dhrystone 1.1 (of course), the 960CF provided a 60% performance boost over a 33-MHz 960CA in a system using 80-ns DRAM (with 2-1-1-1 wait-state performance). For an SRAM-based system (using 20-ns RAMs providing zero-wait-state performance), the 960CF boosts performance by only 15%. The on-chip caches allow the chip to deliver 70,650 Dhrystones in a DRAM-based system—just half a percent below the 70,950 Dhrystones delivered by the SRAM-based system. (For the 960CA, using DRAM instead of SRAM causes performance to drop by 29%.) Of course, some applications won't fit in the on-chip caches as well as Dhrystone, and such applications won't see as big a performance boost.

Samples of the 960CF are available now, with production in the fourth quarter. Pricing in quantities of 10,000 ranges from $105.80 for the 16-MHz version in a PQFP to $165.30 for the 33-MHz version in a PGA.

IBM Announces 100-SPECmark RS/6000

IBM has announced a new top-of-the-line RS/6000 system, the Model 970, offering 100.3 SPECmarks (SPEC89: 49.3 SPECint89, 160.9 SPECfp89; 47.1 SPECint92, 93.6 SPECfp92). This system is the first to use an enhanced version of the processor chip set, implemented in IBM's 0.5-micron CMOS4 process, that provides a 32-Kbyte instruction cache instead of the 8-Kbyte cache in previous implementations. (The instruction cache is limited to a single chip, since it is on the same die with the instruction decoding and dispatch logic.) The data cache is 64K bytes, like other high-end RS/6000 models, and the clock rate is 50 MHz. The 32K instruction cache is initially offered only in a high-end configuration—a rack-mount system with 64 Mbytes of RAM and 2.7 Gbytes of disk, priced at $97,822—but it is likely to find its way into desktop systems before long.

BAPCo Ships PC Benchmark Suite

The Business Applications Performance Corporation (BAPCo) has announced its first benchmark suite, designed to measure stand-alone, single-tasking, x86-based PC performance. BAPCo was founded in May 1991 as a non-profit corporation, and it has been backed by Intel, Dell, HP, IBM, InfoWorld, C&T, Microsoft, NCR, Novell, Lotus, Ziff-Davis, NSTL, and DEC.

The suite is based on 12 real applications, divided into 5 categories: word processing (Word for Windows and WordPerfect), spreadsheet (1-2-3, Excel, and Quattro Pro), data base (dBASE IV and Paradox), desktop publishing (Pagemaker 4.0), software development (Borland C++ and Microsoft C), and graphics (Harvard Graphics). A "workload manager" coordinates execution of each benchmark segment, which consists of loading a script, setting configuration files, running the application using the script, verifying correct results, and reporting the performance measurement. Performance is reported in "scripts per hour," separately for each category and also as a weighted average of all the categories to produce a single metric.

BAPCo represents a big step forward for PC benchmarking, which has been dominated by limited and misleading benchmarks such as Norton SI, Landmark, and PowerMeter. The BAPCo suite shouldn't overrate the value of small caches, as smaller benchmarks do. It is a full system benchmark, incorporating disk and display performance as well as CPU speed. A multitasking benchmark is planned for late this year, with a network benchmark to follow next year.

The BAPCo benchmark suite is sold as a complete product that includes "crippled" versions of all the applications required, so the user does not need to have the applications. The suite costs $795 per copy, and it can be ordered by calling BAPCo at 408/988-7654.

Errata: R4000 SPECint89 is 40.0

Because of a typo, Table 1 on p. 8 of our 5/6/92 issue lists the SPECint89 performance for the R4000-based MIPS Magnum as 30.0, but the correct number is 40.0. The chart on p. 9 of that issue shows the correct value, and SPEC92 figures are shown in the table on p. 12 of this issue.♦