Most Significant Bits

Intel Samples 3.3-V 386SL

Intel has begun sampling a 3.3-V version of the 386SL microprocessor, adding to the 3.3-V 486SX that the company announced in February. The chip will support a mix of logic levels on its interfaces, offering a 3.3-V or 5-V ISA bus interface while providing a 3.3-V DRAM interface. The companion 82360SL I/O chip remains at 5 V for now, as do the keyboard and floppy disk controllers.

The 3.3-V 386SL is priced at $102 in quantities of 1000 for the 20-MHz version; no 25-MHz version is available. A 20-MHz version without cache support is $84, and a 16-MHz version—the first 386SL to be offered at this low a clock rate—is $60, without cache support.

AMD, C&T, and Cyrix have all sampled 3.3-V processors, but no systems are yet in production using them. While Intel is a bit behind in shipping 3.3-V parts, the processors are not the limiting items. DRAMs specified for 3.3-V operation have had very limited availability and high prices, and many other system components, including disk drives and LCD displays, are not yet available in 3.3-V versions. Mixed 3.3/5-V systems should begin shipping this year, with full 3.3-V systems coming on the market sometime in 1993. Such systems will potentially double battery life, at least for systems without backlights.

Vadem Joins Integrated Processor Market

Vadem, a small San Jose-based company that has developed system logic and power management chips for several vendors over the past nine years, has entered the integrated processor market with its VG-230 "Sub-Notebook Engine." The chip is manufactured by NEC, and it was developed using that company's cell libraries. In a 160-pin package, the VG-230 combines a 16-MHz V30HL (8086-compatible) processor, XT system logic, power-management logic, LCD display controller, keyboard scanner, serial port, parallel port (which shares the keyboard scanner pins and is therefore available only if that function is disabled), and PCMCIA memory card interface. LCD displays of CGA resolution and up to 640 × 400 (following the AT&T standard) are supported. The power-management logic is based on Vadem's VG-647, which has been marketed by Intel as the 82347 power-management chip.

The VG-230 is most similar to C&T's PC/Chip, which is likely to be its key competitor. Both devices provide all the functions of a basic PC/XT except memory. The other entrant in this market is NEC's DOS Engine, which Vadem helped design. NEC's chip is less integrated; it does not include a display controller, serial port, or PCMCIA interface.

The VG-230 is priced at $38 in "large OEM quantities." Samples are promised for this month. Both 3-V and 5-V versions are promised. At 5 V and 16 MHz, power consumption is 200 mA maximum.

Intel/AMD Arbitration Ruling Confirmed

On May 22, California Superior Court Judge Read Ambler confirmed the arbitrator's ruling in the AMD/Intel arbitration. (Confirmation by the court is required to make the arbitration ruling legally binding.) Intel opposed the confirmation, claiming that arbitrator Joseph Phelps had overstepped his bounds in awarding AMD immunity from claims of infringement for its Am386 microprocessor. The judge rejected Intel's arguments and ruled that Phelps was within his rights.

One of Intel's objections was that the arbitrator could not preclude a federal court hearing of the issues. Judge Ambler ruled that indeed he could not, and did not, preclude such a hearing; the copyright infringement questions will be heard in federal court, and it is up to that court to decide whether or not to accept the defense offered by the arbitration ruling. Judge Ambler writes, "Intel is as free to institute and prosecute actions as it was before the award. The fact that the arbitrator included precatory language in the award stating his intent that the award of the rights constitute a complete defense that will defeat present and future litigation does not mean that it will have that effect." Thus, the confirmation of the award does not give AMD guaranteed immunity in pending or future litigation, but it is likely to serve as a compelling precedent.

To no one's surprise, Intel is appealing the confirmation of the ruling.

C&T Files Counterclaims Against Intel

Chips and Technologies has filed suit against Intel, claiming that Intel's 386SL violates C&T's patent number 4,924,375, covering a page-interleaved memory access method. This patent has also been asserted against chip-set makers Elite Microelectronics, Suntac, Eteq, and OPTi. The OPTi case has been partially tried, and although one of OPTi's older products was ruled to be infringing, a key current product was deemed non-infringing.

C&T's suit also revisits the often-made charges that Intel's "Palmer" patent, which covers certain aspects of math coprocessor designs, is invalid because Intel allegedly "willfully concealed relevant information and otherwise misled the Patent and Trademark Office when

applying for the patent." C&T has lots of friends in attacking this patent; in addition to C&T, Intel is suing Cyrix and ULSI Systems Technology for allegedly infringing this patent, and both companies make similar arguments concerning the validity of the patent. This is a critical patent not just because of the 387 market, but also because any full 486 implementation must also include the FPU and thus potentially violates this patent, if it is upheld.

C&T furthermore claims that Intel "has made false and misleading statements about the alleged infringement of Intel's patents by CHIPS' products." Finally, C&T filed counterclaims to Intel's suit against them, claiming to show that its Super386, PC/Chip, and Super387 products do not violate Intel's patents.

This countersuit is the obvious counterattack for C&T to make, and the court will have to decide whose arguments are right. The attack on the 386SL is clearly a bargaining chip, similar to Hitachi's patent infringement claim against Motorola's 68020 that served as a key element in Hitachi's defense against Motorola's claim that the H8/500-series processors infringed Motorola's patents.

PowerPC On Track, Names Revealed

Last month, IBM, Motorola, and Apple formally dedicated their joint design center, named Somerset, and used the occasion to wave the flag for the PowerPC alliance. Despite widely reported comments that they were ahead of schedule, the dates they gave were essentially the same as those given at the Microprocessor Forum last November.

Virtually the only new information provided was the part numbers for the four devices that previously have been discussed only under generic names. (See µPR 12/26/91, p. 1 for a general description of the chips. No further information has been released.) The initial "low-cost desktop" chip, which is derived from IBM's single-chip RS/6000 implementation used in the model 220, will be called the 601. This chip is "very close" to taping out, and samples are promised by the end of the year. The "portable computer" chip will be called the 603 (begging the question of what the 602 is), and the "mainstream desktop" chip will be the 604. These two chips are expected in late '93. The high-end workstation and server chip, due in '94, will be the 620, leaving plenty of unused numbers in-between.

IBM will continue developing multichip implementations of its POWER architecture, but these designs will be limited to the very high end of the product line. IBM plans to base all of its mainstream workstation products on the PowerPC chips. Apple will build machines at lower price points than IBM's, and Apple will focus on a PowerPC port of System 7, rather than the PowerOpen UNIX environment that IBM will use.

Both Bull and Thomson-CSF have signed up to build systems using the PowerPC chips. Neither deal includes the right to sell chips on the merchant market, however. While the contracts between Apple, IBM, and Motorola have provisions for an alternate source, none is expected soon.

Siemens Unveils Enhanced Microcontrollers

Siemens has announced a new 8052-compatible microcontroller based on a 40-MHz CPU core. The SAB C501 is available with 256 bytes RAM in ROM-less and 8K ROM versions. It will cost $3.50 in 10K-unit quantity, and it is sampling now with production availability scheduled for third quarter. At the same time, Siemens announced two other 8052-compatible products, the SAB C502 and SAB C503. Available at speeds up to 18 MHz, the C502 features 16K ROM and 512 bytes RAM while the C503 offers 8K ROM, 256 bytes RAM, and an 8-channel, 10-bit A/D converter. Both parts have two watchdog timers, and are available in ROM-less and EPROM versions. The SAB C502 will cost $5.50 in 10K quantity, and it is expected to be sampling in fourth quarter with production availability in the first quarter of 1993. The SAB C503 will cost $4 in 10K quantity, with samples available now and production planned for fourth quarter.

An upgraded version of Siemens' 80C166 16-bit microcontroller (see µPR 3/7/90, p. 8) was also announced. The SAB 80C167 offers faster interrupt processing, larger RAM (2K bytes) more parallel I/O (110 lines), more A/D channels (16), more capture/compare channels (32), and additional instructions. Available with 8K ROM, the 80C167 will cost $30 in 10K quantity. Samples are expected in third quarter with production availability in the first quarter of 1993.

EFAR Microsystems Enters Chip-Set Market

The most recent entrant in the PC chip set market is San Jose-based EFAR Microsystems, offering their EF8290WB chip set for 386DX and 486 system boards. EFAR's 82EC392 bus controller and 82EC495 system controller are pin- and BIOS-compatible with OPTi's popular 82C392 and 82C493 chips for AT-compatible system boards with cache. EFAR's chip set costs $24 in 100-unit quantities. Samples are available now, and volume production is planned for this quarter.

This is actually the second chip set designed for compatibility with OPTi's 82C391/493, the first being Micro Integration's MIC9392 and MIC9493. The latter is enhanced with the ability to interleave DRAM banks of different sizes, which is automatically invoked whenever possible without requiring a customized BIOS. (OPTi and EFAR don't support interleaving.) ♦