Resources

Selected DECWRL Papers

As noted in the article on page 14, DEC's Western Research Laboratory has published a variety of technical papers during its 10-year history. The table shows a few of the processor-related papers:

To order, request an order form from Technical Report Distribution, DEC Western Research Laboratory, WRL-1, 250 University Avenue, Palo Alto, CA 94301, or send e-mail to: WRL-Techreports@decwrl.dec.com.

Report Number	Title	Authors
86/1	Titan System Manual	Michael J. K. Nielsen
87/1	The Mahler Experience: Using an Intermediate Language as the Machine Description	David W. Wall and Michael L. Powell
87/4	Cache Coherence in Distributed Systems	Christopher A. Kent
87/8	MultiTitan: Four Architecture Papers	Norman P. Jouppi, Jeremy Dion, David Boggs, Michael J. K. Nielsen
89/7	Available Instruction-Level Parallelism for Superscalar and Superpipelined Machines	Norman P. Jouppi and David W. Wall
89/9	Architectural and Organizational Tradeoffs in the Design of the MultiTitan CPU	Norman P. Jouppi
89/10	Integration and Packaging Plateaus of Processor Performance	Norman P. Jouppi
89/13	The Distribution of Instruction-Level and Machine Parallelism and Its Effect on Performance	Norman P. Jouppi
89/14	Long Address Traces from RISC Machines: Generation and Analysis	Anita Borg, R.E. Kessler, Georgia Lazana, and David W. Wall
91/7	Pool Boiling on Small Heat Dissipating Elements in Water at Subatmospheric Pressure	Wade R. McGillis, John S. Fitch, William R. Hamburgen, Van P. Carey
91/10	Experience with a Software-Defined Machine Architecture	David W. Wall

Fourth Annual Hot Chips Conference

The IEEE-Sponsored Hot Chips conference will be held August 10 and 11 at Stanford University. The highlight of the program is a preview of Intel's P5. The program includes presentations on many of this year's high-performance microprocessors, including the 21064 Alpha chip, PA-RISC 7100, LSI's 33020 X terminal controller, hyperSPARC, and the ARM600. Also included are sessions on low-power systems, multiprocessor interface

issues, interface and interrupt chips, vector processors, and an evening panel session on new DRAM alternatives. In addition to the main conference program, Prof. Mark Hill from the University of Wisconsin, Madison will present a half-day tutorial on August 9, titled *A Quantitative Approach to Microprocessor Architecture*.

Registration for IEEE members is \$170 if postmarked by July 15, or \$240 thereafter; nonmember prices are \$240 and \$290. Registration for the Sunday tutorial is an additional \$10. VISA and MasterCard are accepted. To register or request a program brochure, write to Hot Chips, c/o Dr. Robert G. Stewart, Stewart Research Enterprises, 1658 Belvoir Dr., Los Altos, CA 94024; fax 415/941-5048; email r.stewart@compmail.com. ◆

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