Most Significant Bits

Intel Demos P5, Sets 1Q93 Intro Date

Breaking its official silence on the status of the P5, Intel last week demonstrated a P5-based system for reporters and revealed that the introduction of the chip has been delayed until the first quarter of next year.

Intel claims that the chip is now running hundreds of applications under DOS, Windows, OS/2, and UNIX, and that alpha testing has been completed. Beta-test samples will be distributed to a broader group of system makers in the coming months. Intel VP Paul Otellini conceded that there are some bugs, as expected at this stage in the chip's evolution, and he said that three teams of engineers are working around-the-clock to correct them.

With the 486, Intel announced the chip at spring Comdex in April, 1989, but full production did not begin until late that year and serious bugs were found as late as November. With the P5, Intel wants to delay the introduction until volume production has begun and system vendors are ready to ship products. They also want to make sure that the chip is as bug-free as possible before they put it into production, hoping to avoid the repeated crises that plagued early 486 production.

Technical disclosures will be made and systems demonstrated well in advance of the introduction, making the introduction itself just an announcement of price, availability, and presumably the name (which is now expected *not* to be 586). The motivation for the delayed introduction is, in part, to make the chip announcement most effective for the system makers, who don't like early announcements that could suppress demand for existing products and create desire for products they can't ship yet. Intel's strategic need to convince the world that the P5 is coming along well has been met with the limited disclosure and demonstration that have been done.

Some question remains about how much of a delay in production the shift represents. Intel has, in the past, said that systems would ship in late '92, so there does seem to have been a slip of a few months. Given the complexity of the chip, it would almost be more surprising if there were *not* such a slip.

Intel says that demand for 486DX-50 and 486DX2 processors is well above expectations, and this could be part of the motivation for slowing down the P5 production ramp. The P5 will be built on the same 0.8-micron production lines as the 486DX-50 and 486DX2 (with a few extra steps since the P5 is BiCMOS), and Intel may be hesitant to take production capacity away from these product lines.

Intel did not reveal any new technical details, saying that they cannot do so until all the European patent applications are filed. Paul Otellini did say that he expected 66 MHz to be the lowest frequency offered, and that the performance goals of two times the 486 at the same clock rate (for integer code) and 100 MIPS (based on Dhrystone 1.1) had been achieved. Floating-point benchmarks were not complete, he said, but the goal remains five to seven times the performance of the 486. These speed-ups are for code that has been recompiled for the P5, and it is not clear how much slower the P5 will be for existing 386 and 486 binaries.

Intel Forges 386SL Deal With VLSI Technology

Intel has entered into an agreement with VLSI Technology to develop 386SL derivatives for the emerging "pocket intelligence" market. In addition to the joint development plans, Intel is investing about $50 million for just under 20% of VLSI Technology, giving VLSI the capital it needs to aggressively pursue this opportunity. VLSI has established the Portable Systems Division for this effort.

AMD reportedly tried to buy VLSI Technology earlier this year, and some analysts suspect that Intel's interest in doing a deal with VLSI was partly influenced by a desire to keep AMD out.

According to Mike Aymar, VP of Intel's Entry-Level Products Group, Intel believes that the emerging palmtop/personal intelligence market represents an enormous growth opportunity, and that it is especially important as the PC market matures and becomes a replacement market with slow growth.

Intel believes that the need for high integration and product differentiation will dictate the use of customized chips for this market. Intel's design tools—while very powerful for designing large, very complex chips—are not well suited to crafting numerous customer-specific variations. According to Aymar, Intel therefore sought a partner to provide this design capability. Intel does not plan to develop its own standard products for this market. VLSI's COMPASS ASIC design tools are widely regarded as among the best in the industry, and the company also has a successful PC chip set line and all the library elements needed (except, until now, for the processor core) for PC-compatible systems.

In making this alliance, Intel is hoping to shore up its position against Hobbit and ARM in this emerging marketplace. As noted in last issue's editorial, this market will be driven by an entirely new set of application programs and operating systems, making the PC momentum of the x86 less valuable. The chips resulting from the Intel/VLSI alliance seem destined to be significantly slower than the Hobbit and ARM devices, which

may or may not be a serious disadvantage. It remains to be seen how power consumption, integration level, and price will compare.

What VLSI will get from Intel is the 386SL core CPU—not the cache controller, AT bus interface, or peripherals. The 386SL core is being used instead of the 386SX because it is a static design and includes system management mode for power management. While the 386SL is currently manufactured in 1-micron CMOS, the core is being reimplemented in Intel's 0.8-micron, three-level-metal process, now used for the 486DX-50 and the 486DX2.

VLSI Technology is converting its library of functional blocks into VHDL models, which will ease their implementation on Intel's process. Intel is providing the a behavioral model for the 386SL core. Modifications to the core are not allowed.

Intel and VLSI are visiting customers jointly, and both will work with software developers, content providers, and other key players needed to support the architecture in this application area. VLSI has responsibility for working with customers to define custom devices using the 386SL core, and the chip design will be done by VLSI's own staff. (The 386SL core will not become part of VLSI's standard ASIC library.) Intel will manufacture all chips that include the 386SL core, and VLSI will build any support chips. VLSI Technology will have exclusive rights to sell the resulting devices.

While the design of the first product is still in flux, VLSI expects to start with a two-chip set: one chip that includes the 386SL core, and another that includes a display controller (based on Weitek's accelerated VGA-compatible controller, which VLSI recently licensed). The two-chip set will presumably include basic PC system logic and some I/O ports. Samples are expected in the second quarter of 1993, with production in the third quarter. In future designs, VLSI plans to include dedicated hardware for handwriting recognition using fuzzy logic technology it has licensed from Togai Infralogic.

This arrangement gives VLSI a limited role, since it will not be doing any CPU manufacturing, cannot modify the core, and does not have access to any other Intel cores. VLSI is not allowed to pursue traditional PC or notebook computer applications. Furthermore, the joint program is intended to produce customer-specific devices, and there are no immediate plans for standard devices. Standard chips are not precluded, however, and if VLSI and Intel find enough commonality in the needs of many customers, a standard product could be offered. Such a product would be sold by VLSI Technology, even though it would be manufactured by Intel.

VLSI Technology is now in the midst of two competing camps in the pocket intelligence market; it has been making ARM chips for Apple, and it will continue to do so. VLSI will not, however, promote the ARM processors for portable computing applications; the company's strategic focus—no doubt driven, in part, by Intel's $50 million—is on 386SL-based products.

The ARM designs are created by ARM, Ltd. in England, and GEC Plessey also manufactures them, so the shift of priorities at VLSI shouldn't have much impact on Apple. It is worthy of note, however, that VLSI apparently did not deem the Newton-based market (beyond Apple) worthy of pursuing. Apple, incidentally, is VLSI's largest customer; every Macintosh has at least one VLSI ASIC in it.

AT&T and Go Announce Alliance

Just days after the Intel/VLSI announcement, AT&T and Go formally announced their alliance to port Go's PenPoint operating system to AT&T's Hobbit microprocessor. This is the first public sign of a major effort underway at AT&T to take a leadership role in the personal communicator market. AT&T has formed a new business unit, called Personal Communication Systems and located in Sunnyvale, CA, to focus on this market.

Very few details were given; no specifics were provided on the Hobbit microprocessor, and no mention was made of EO Computer, the GO spinoff that is believed to be developing a Hobbit-based personal communicator with AT&T funding. (See µPR 2/12/92, p. 1 for an overview of Hobbit's history and architecture.)

Until now, GO's operating system has been available only for the 386 architecture. Most of the 8.5" × 11" pen-based computers now on the market can run either PenPoint or Microsoft's Pen Windows, and machines of this class are likely to stick with the x86 architecture because of the flexibility it provides to run existing PC software (with pen adaptations). For the hand-held device market, however, the x86 software base is of little value, and it is in this market that Go expects Hobbit to flourish.

While Hobbit could, in theory, be used for pen-based devices that lacked communication capabilities, AT&T is focusing specifically on communications-oriented products. (Low-cost devices might not have wireless communications links, but all are likely to have at least a telephone line connection.) AT&T has considerable expertise in the communications infrastructure, of course, and it has also developed a variety of communications-oriented chips. Although the initial Hobbit chip probably won't have any communications-specific features, AT&T plans to integrate a DSP core and other functions on the same chip as the processor, working toward a single-chip personal communicator.

A general overview of the Hobbit chip set will be presented at the Hot Chips conference in August; full details of the processor chip will be unveiled at the Microprocessor Forum in October.♦