THE EDITORS' VIEW

Speed Kills? Not for RISC Processors

Cost of Complexity Becomes Clear from SuperSPARC, 88110

As we watch the parade of superscalar and superpipelined microprocessors, we see that there are two distinct schools of thought regarding the design of such chips. One group—exemplified by IBM, Sun, and Motorola—holds that performance increases come from improving the IPC, or instructions per cycle. We will call this group the Brainiacs. The other—MIPS, HP, and DEC—believes that clock rate is still the key, and the complexities of multiple instruction issue are good only so long as they do not hinder high-speed designs. These are the Speed Demons.

One might think that this tradeoff simply reflects the preferences of the designers and that both techniques can be used to achieve high performance. The facts, however, do not support this theory. The top performing microprocessors shipping today, based on SPECint92, are DEC's 21064, HP's PA7100, and the MIPS R4000. The latter chip edges out IBM's RIOS for third place, even though the R4000 has been shipping for a year and uses one rather than three chips.

The Speed Demons have gained this performance edge by racing to a large advantage in clock speed over the Brainiacs. At 99 MHz, HP is the slowest of the three Speed Demons, while IBM, the fastest of the Brainiacs, tops out at just 62.5 MHz. This gap is too wide to be breached simply by increased parallelism; although IBM's processor is 20% more efficient in SPECint92 per MHz, the HP design achieves a 60% higher clock rate. Using the same measure, SuperSPARC is 3× more efficient than the 21064, but the DEC clock is 5× faster.

The situation changes little if we examine floating-point performance. Although the IBM chip set does greatly exceed the R4000 in this area, this is primarily due to MIPS' decision not to emphasize floating point in its design. The two top floating-point chips are still from HP and DEC, in the Speed Demon camp.

The Brainiac marketing departments are working overtime to hide their disadvantage. IBM, for one, likes to show graphs comparing its "efficiency" against other microprocessors. The fallacy of this tactic is that it removes clock frequency from the comparison, as if vendors could simply "turn up the clock" whenever they want. Unfortunately, they cannot, despite their best efforts. TI, for one, is working desperately to push SuperSPARC beyond 40 MHz, so far to no avail. Motorola is hard-pressed to reach 50 MHz with its 88110.

The complexity of the Brainiac chips creates many obstacles against increasing the clock. In the case of IBM, the circuitry needed to implement its four-way superscalar design could not fit onto a single chip, and in fact ended up as a three-chip processor. The added time needed to send signals between chips has been one factor limiting the clock rate of RIOS.

SuperSPARC's low clock rate comes, at least in part, from a complicated cache structure that must provide data twice per clock cycle, and cascaded ALUs that perform two dependent operations per clock. Motorola hasn't discussed critical paths in the 88110, but the history buffers and scoreboarding required by speculative and out-of-order execution may be a problem.

Another cost of complexity is its impact on design time. In a market where performance is increasing by 5% per month, a six-month slip can make a new CPU suddenly uncompetitive. Had SuperSPARC shipped in 1991 as originally planned, it would have been a strong product, but by 1992 it fell behind the power curve. In 1993, Sun is struggling to ship 40-MHz systems, despite its original plans to start at 50 MHz.

The 88110 has had similar schedule problems, taking well over a year after first silicon to reach production. IBM has been working on its RIOS 2 design for three years and products are just now appearing on the distant horizon. By contrast, HP was able to ship the PA7100 just 15 months after its earlier Snakes design. The R4400 provides a 50% performance boost over its predecessor in a similarly short period.

The Speed Demons have their own problems. High clock rates increase heat dissipation; the Alpha chip can generate up to 28 watts. Some designs require fast, expensive SRAMs to reach their peak performance. System vendors appear to be able to solve these problems and use these speedy chips to deliver higher performance to their customers.

The Brainiacs seem to be set in their ways; IBM's RIOS 2 design looks amazingly like its RIOS 1 design. The Brainiacs have even welcomed a new member, as Silicon Graphics has taken the complex approach with its forthcoming TFP processor. (Its MIPS Technologies subsidiary, however, continues to follow the clock rate path with the R4000 family.) Although IBM has the packaging and process technology to make nearly any design tactic succeed, Sun and SGI may need to take a more competitive approach. ♦