Literature Watch

ASICs

Alterable RISC core fine tunes ASIC architecture. *ASIC design library eases complex chip design with malleable blocks and predefined silicon to cut time to market.* Dave Bursky, Electronic Design, 2/4/93, pg 92, 2 pgs.

Don't take 3-V ASICs for granted. *Applying 5-V ASIC library cells in 3-V designs requires careful navigation through numerous obstacles.* Bill Feger, AT&T Bell Laboratories, Electronic Design, 1/21/93, pg 47, 6 pgs.

Buses

Hardware/software issues highlight conferences. *SCSI-3 scores at Buscon, while Softcon pulls in the real time embedded software topics system integrators crave.* Richard Nass, Electronic Design, 2/4/93, pg 39, 6 pgs.

Development Tools

Boost programmable logic performance with timing driven tools. *The best way to avoid timing problems at the end of a design is to use tools and methods from the start that help you meet your timing constraints.* Doug Conner, EDN, 2/4/93, pg 47, 6 pgs.

DSPs

Although multimedia drives DSP system boards, instrumentation-grade products don't lag behind. *This article examines recent products for IBM class machines by the DSP chip they use.* Paul G. Schreier, Personal Engineering & Instrumentation News, 2/93, pg 44, 9 pgs.

Roll your own TI DSP chip: combine a C25 and 15k-gate array. *You can roll your own DSP chip with the TI TEC320C25A, which combines a C25 DSP µP with a 15k-gate array and 1K × 16-bit programmable RAM. Also added are clock PLL power-down mode and serial pseudo-ICE control for debugging.* Ray Weiss, EDN, 2/4/93, pg 65, 2 pgs.

Memory

Flash future bright, despite shortage. Jeffrey Child, Computer Design, 2/93, pg 93, 4 pgs.

Miscellaneous

The humbling of T.J. Rodgers. *Silicon Valley's iconoclast sees his company suffer a mid-life crisis like other semiconductor companies as sales decline for the first time and a fab is closed.* Robert Ristelhueber, Electronic Business, 2/93, pg 30, 6 pgs.

Talking heads. *When you really want to know what's happening, ask the people who are calling the shots: the Chief Executive Officers. We decided to do just that by asking the CEO's from the leading pen operating environment companies about the future of pen computing: Bill Gates, Microsoft; Jerry Kaplan, GO; James Dao, CIC; Bruce Walter, GRiD Systems; Jin Kim, PI Systems; Brian Daugherty, GeoWorks*. Pen Magazine, 1/93, pg 34, 6 pgs.

The Smart House system: a technical overview. *There are a number of home automation technologies vying for market share. Smart House was developed as a proprietary system initially aimed at new construction. Find out just what makes Smart House tick.* H. Brooke Stauffer, The Computer Applications Journal, 2/93, pg 14, 7 pgs.

Adaptive fuzzy systems. *By reorganizing themselves internally as appropriate, these fuzzy control systems can function within a changing external world.* Earl Cox, Metus System Group, IEEE Spectrum, 2/93, pg 27, 5 pgs.

Communications terminals get personal. *Personal communication systems (PCSs) are stymied only by a lack of assigned frequency spectrums.* Milt Leonard, Electronic Design, 2/4/93, pg 61, 6 pgs.

Peripheral Chips

DSP technique nearly doubles disk capacity. *A digital scheme can jettison most of a read channel's analog circuits that routinely capture hard-disk digital data.* Frank Goodenough, Electronic Design, 2/4/93, pg 53, 5 pgs.

Video teleconferencing pushes video chips to their limit. *Synchronization and image compression are the key IC technologies for putting video-in-a-window on PCs.* Stephan Ohr, Computer Design, 2/93, pg 49, 6 pgs.

Processors

Digital's Alpha chip project. *Alpha was the largest engineering project in Digital's history, spanning more than 30 engineering groups in 10 countries. These articles explore some of the critical technical areas involved in bringing the product set from concept to reality: architecture, semiconductors, hardware, operating system, and migration.* Robert M. Supnik, R.L. Sites, et al, Digital Equipment Corp.; Communications of the ACM, 2/93, pg 30, 52 pgs.

Programmable Logic

Wes Patterson on PLDs and FPGAs. Wes Patterson, Xilinx, Computer Design, 2/93, pg 25, 3 pgs.

FPGAs achieve PAL-device figures. *The Actel 0.8-µm Act 3 family of FPGAs achieves a clock-to-output delay of 10 nsec. The five devices have 1500- to 10,000-gate densities and can accommodate designs having 125-MHz internal clock rates.* John Gallant, Actel Corp.; EDN, 2/4/93, pg 60, 1 pg.

