Most Significant Bits

NEC Introduces VR3800 for Embedded Control

Japanese giant NEC jumped into the market for MIPS-based embedded control chips by announcing its VR3800 processor. The new chip combines an R3000A CPU core with 4K of instruction cache and 1K of data cache. To further reduce system part count, the NEC design also includes a PLL to generate all of the clocks needed by the R3000 core as well as the standard write buffer circuitry usually implemented with an R3020 or equivalent part. It will be available at 16, 20, and 25 MHz.

NEC had been focused on the mainstream R3000 and R4000 market while its smaller American rivals—IDT, LSI, and Performance Semiconductor—pursued embedded designs with their own derivative MIPS-based CPUs. With the VR3800 and future follow-ons, NEC can now compete for applications such as laser printers and X-terminals. The company expects to sample the VR3800 in 2Q93 with volume production in the following quarter. Sample prices range from $40 to $49 (depending on frequency) and NEC says they should fall by about 20% for volume shipments.

Thomson Announces First PowerPC Product

Cetia, a subsidiary of Thomson-CSF, jumped the gun to become the first company to announce products based on the still-unannounced PowerPC 601 processor. The French firm will ship a family of VME boards under the name Power Engine, starting in September. The first two products are single-board computers designed to run either a version of IBM's AIX operating system or LynxOS, a real-time operating system. They can also be configured in a two-processor arrangement. Future products in the family will include a graphics board.

The announcement itself was rather vaporous, as the company would not provide specific information on pricing, performance, or configurations. Pricing was said to be comparable to 68040-based products, and the performance estimates were the same as those given at the last Microprocessor Forum. Motorola promises that measured performance will be disclosed when the 601 begins general sampling next quarter.

Carrera Ships R4000 Board for Windows NT

Carrera Computers (Laguna Hills, CA) hopes that the nascent Windows NT market will provide an opportunity for RISC to gain a foothold in the PC business. The startup company announced its Cobra ARCSystem motherboard, based on the R4000, for NT systems. The board retails for $4995 and includes a 50/100 MHz R4000PC CPU, a SCSI-2 interface, an Ethernet port, a 1280 × 1024 × 8 graphics accelerator, four EISA slots, and other standard motherboard hardware. It is based on MIPS' ARCset design *(see **060601.PDF**)*.

Although Carrera touts its board as the first 64-bit PC motherboard, in fact Windows NT will not take advantage of the 64-bit features of the CPU. Carrera claims that the board runs NT three times faster than a 50-MHz 486, although the SPECint92 rating of the MIPS chip is only about 40% faster. Until real benchmarks on a real version of NT are available, it will be difficult to verify such performance claims.

MIPS Opens Design Center for NT Systems

While a few companies like Carrera have forged ahead with designs based on the ARCset, most PC companies have found that design too complicated and too expensive for the PC market. To address this problem, MIPS Technologies has created its Open Design Center (ODC) to assist companies in building Windows NT systems using the R4000 and R4400. The ODC sells and supports a set of low-cost design kits that allow these companies to design these systems quickly.

To reduce the cost of the initial ARCset and take advantage of the low cost of standard PC technology, MIPS has designed two ASICs that connect its R4000-family processors to a 486-style local bus. Using these chips, a designer can easily replace a 486 processor with a MIPS processor and still use the same memory, graphics, and I/O devices. These ASICs will be available from multiple vendors with an approximate price of $30 in volume. MIPS estimates that only 10%–15% performance is lost by interfacing to standard PC components, but no benchmarks are available to validate this claim.

Through the ODC, MIPS will provide not only the system logic chips but complete system design kits, including schematics, drivers, diagnostic code, and HAL (hardware abstraction layer) code to interface with Windows NT. Two of the designs interface an R4x00PC processor with ISA or EISA systems. A third uses a R4x00SC processor with secondary cache to achieve higher performance. MIPS also plans to have a VL-Bus interface by the end of the year, and a PCI interface in early 1994.

The design kits cost just $5000 each in up-front fees, plus a $10 per unit royalty for the software. This is a huge change from MIPS initial ARCSystem license, which cost $500,000. By dropping the cost to just a nominal support fee, MIPS hopes to attract a large base of system and component vendors, something the original license scheme failed to establish.

As part of the announcement, Acer indicated its support for the ODC and plans to announce a MIPS-based PC concurrent with NT availability. The company is not using one of the standard designs but has imple-

mented its own chip set that it says will offer higher performance. Acer will make this chip set available to other system vendors on its own and through the ODC. Acer did not reveal any details of its chip set or indicate pricing or availability. MIPS hopes that the ODC will jumpstart a clone market, encouraging other companies to join Acer in offering system components.

MIPS ABI Reaches Fruition

Meanwhile, on the UNIX side of the ranch, the Indians have taken the fort. The original Apache group, renegades in the ACE consortium because they believed in big-endian systems running the SVR4 version of UNIX, have now established the official application binary interface (ABI) for MIPS-based UNIX systems. This ABI ensures that software vendors can develop applications on one MIPS platform and have confidence that the same binaries will work correctly on systems from a variety of vendors. Companies announcing that their systems will support the new ABI (with shipment dates as indicated) are Control Data (now), NEC (now), Tandem (now) Pyramid (March), Silicon Graphics (May), Siemens-Nixdorf (mid-93), Sony (mid-93), and Concurrent Computer (early 1994). Other system vendors supporting the initiative include Olivetti and AT&T.

These companies have been working on the specification for nearly a year. In addition to the system vendors, key ISVs such as database vendors Oracle and SAS also contributed to the development process. The MIPS ABI is built on top of the generic ABI (gABI) specified by UNIX System Laboratories (USL) for its SVR4 release. The new specification includes the X11 and Motif graphical standards and other extensions to the gABI.

The group selected the MIPS Magnum 3000 workstation as the reference platform for the ABI. Thus, the standard is based on the older R3000 processor. This choice reflects the fact that the bulk of the installed base has not yet migrated to the 64-bit R4000. The group is currently working on extensions to the ABI for the R4000 and other future MIPS processors.

Establishing a standard ABI became much easier once DEC lost interest in the MIPS architecture. DEC was the leading promoter of the little-endian, OSF-based standard that ACE selected, but most of the other system vendors in ACE use big-endian designs with SVR4. With DEC now pursuing its Alpha strategy, these other vendors were able to come to an agreement quickly.

This announcement brings the MIPS architecture to par with other popular RISC architectures by establishing a single standard to which software developers can code. Other processors have a single dominant player that has established a *de facto* software standard, but MIPS system shipments have been fragmented among a number of vendors. As ISVs make their applications available over the entire breadth of MIPS-based systems, users of these systems should see increased software availability.

SI Launches SPARCware ABI

SPARC International (SI) announced a new SPARCware program to promote a unified ABI for SPARC systems. The ABI, codified in SPARC Compliance Definition 2 (SCD 2), is based on USL's SVR4 gABI and other popular UNIX standards. From a programmer's standpoint it is quite similar to the MIPS ABI, although, in a concession to Sun, it includes the OpenLook interface as well as Motif.

Instead of using a single reference platform, SCD 2 relies on an extensive software test suite to ensure the compliance of both systems and applications. SI will certify software applications at no charge for any ISV. If an application works on one compliant system and not on another (because of a hole in the test suite), systems from Sun and Fujitsu are considered to be reference platforms, and other systems must conform to their behavior.

SI hopes the ABI will make it easier for ISVs to port their applications, not only to Sun systems but to other SPARC systems as well. The group will also spend $2.5 million to promote the SPARCware concept.

Unlike the MIPS scenario, the vast majority of SPARC systems are already being shipped under a single ABI: Solaris on SPARC. Thus, the program is unlikely to attract many new ISVs, since the incremental number of systems is small. The greater benefit is to SPARC vendors such as Fujitsu, HaL, Cray, and Solbourne that don't use Solaris, as SPARCware should give them access to more applications without paying large porting fees.

LSI Announces Faster SBus Controller

LSI Logic announced a new DMA controller, the L64864, for SBus systems. The '864 has a peak transfer rate of 25 Mbytes/s—double the rate of the previous-generation L64854—when connected to 16-bit devices such as LAN or SCSI interfaces. The new chip also adds a new 32-bit mode that can transfer data at up to 100 Mbytes/s, the peak speed of a 25-MHz, 32-bit SBus.

For motherboard applications, the chip can be used in "Mode 1" to control two 16-bit interface chips as well as an 8-bit standard I/O bus. Since other vendors offer lower-cost solutions for standard peripherals, the LSI chip may be more useful in systems that require higher performance or more unusual interfaces than are included in these highly-integrated competitors.

The '864 is better suited for vendors of SBus add-in cards. In the higher-speed Mode 2, it can control a single 32-bit device. This mode is intended for high-speed devices such as SCSI-2, ATM, or HIPPI interfaces. At $79 in quantities of 100, the LSI chip allows third-party vendors to quickly and inexpensively design high-performance SBus cards for these new devices.♦

