Pentium Chip Sets Poised For Launch

Intel and VLSI Pursue PCI, While OPTi Favors VL-Bus

By Mark Thorson and Michael Slater

The introduction of Intel's Pentium *(see **070401.PDF**)* has sent PC-compatible chip set makers scrambling to come up with new high-end desktop solutions. First out of the chute are Intel (naturally), OPTi, and VLSI Technology. Both Efar Microsystems and Silicon Integrated Systems indicated that they have products under development but were unable to provide further information at this time.

While the chip sets announced to date are designed for uniprocessor systems, both Corollary and LSI Logic's Headland Technology division have outlined plans for chip sets supporting multiprocessor Pentium systems.

Pentium system designers face certain challenges, the most difficult being the 66-MHz clock speed. (A 60-MHz Pentium will be available, but all of the first crop of chip sets are planned for availability at 66 MHz.) Unlike the 486DX2-66, the CPU's external bus runs at the full CPU clock frequency, not half that rate.

From the architectural viewpoint, the most significant difference from 486 systems is Pentium's 64-bit data bus *(see **070502.PDF**)*. All of the announced chip sets support 64-bit data paths both to an external second-level cache and to DRAM.

Table 1 compares the announced PC-compatible chip sets for Pentium microprocessors. Note that Intel's chip set is available for either ISA or EISA systems.

The announced chip sets all support some form of standard local bus for adding optional high-bandwidth peripherals, such as video controllers. These can be on-board peripherals or add-in cards. The Intel-originated PCI bus is supported by the Intel and VLSI chip sets, while the OPTi design uses VESA's VL-Bus. OPTi plans to introduce a PCI-based solution next quarter. *(See **060902.PDF** for a discussion of local bus standards.)*

Intel 82430 Provides PCI Support

Intel's 82430 chip set was described in more detail last issue *(see **070403.PDF**)*. It implements PCI as a mezzanine bus between the processor bus and the expansion bus. Three chips—the 82434LX cache/DRAM controller and two copies of the 82433LX data buffer—implement the CPU-cache-DRAM core with a PCI interface, while the 82375EB bus bridge implements the PCI-to-EISA interface.

This is similar to Intel's 82420 chip set for 486-based AT-compatible systems *(see **061602.PDF**)*. The ISA version of the 82430 replaces the 82375EB with the 82378IB bus bridge, first introduced in the 82420 chip set. Both types of bus bridge chips contain on-chip expansion-bus buffers, which contribute to a low glue-logic count. (The ISA bridge contains the standard ISA peripherals and the ISA bus controller; a separate peripherals chip is used with the EISA bus bridge, due to the higher complexity of the peripheral set defined in the EISA standard and the higher complexity and pin count of the EISA bus controller.)

Intel's cache implementation on the 82430 is unique in that it combines on-chip tags with a direct-mapped cache controller supporting either write-through or write-back modes. This is significant because external tag SRAMs would require higher speed than data SRAMs; at 66 MHz, moving the tag SRAMs onto the chip eliminates a major design headache (i.e., at least one chip-to-chip crossing in the critical path) in addition to reducing the total system chip count. External data SRAMs are required, which can be either standard SRAMs used with an external address latch or the newer synchronous (burst-mode) SRAMs.

The cache controller supports 3-2-2-2 burst performance (i.e., 3 CPU clock periods for the first 64-bit data transfer of a burst read, and 2 cycles for each subsequent

Vendor	Chip Set Name	Local Bus	Expansion Bus	Packages	Cache Size	Cache Type	Max DRAM Size	DRAM Bank Depths	Price (1K)	Availability
Intel	82430	PCI	EISA, ISA	(2) 160-pin PQFP, (2-3) 208-pin PQFP	256K, 512K	WT, WB	192M	256K, 1M, 4M	$84 (ISA), $108 (EISA)	Samples—Now Prod.—5/93
OPTi	PTMAWB-V	VL-Bus	ISA	84-PLCC/ 100-PQFP, 160-PQFP, 208-PQFP	64K–2M	WT, WB, AWB (see text)	128M	256K, 512K, 1M, 2M, 4M, 8M	$75	Samples—Now Prod.—Now
VLSI Tech	VL82C580	PCI	ISA	(2) 144-PQFP, 168-PQFP, 208-PQFP	256K, 512K	WT	1G	256K, 1M, 4M, 16M	$65	Samples—3Q93 Prod.—4Q93

Table 1. Intel, OPTi, and VLSI Technology are the only companies to announce price and availability for Pentium system-logic chip sets.

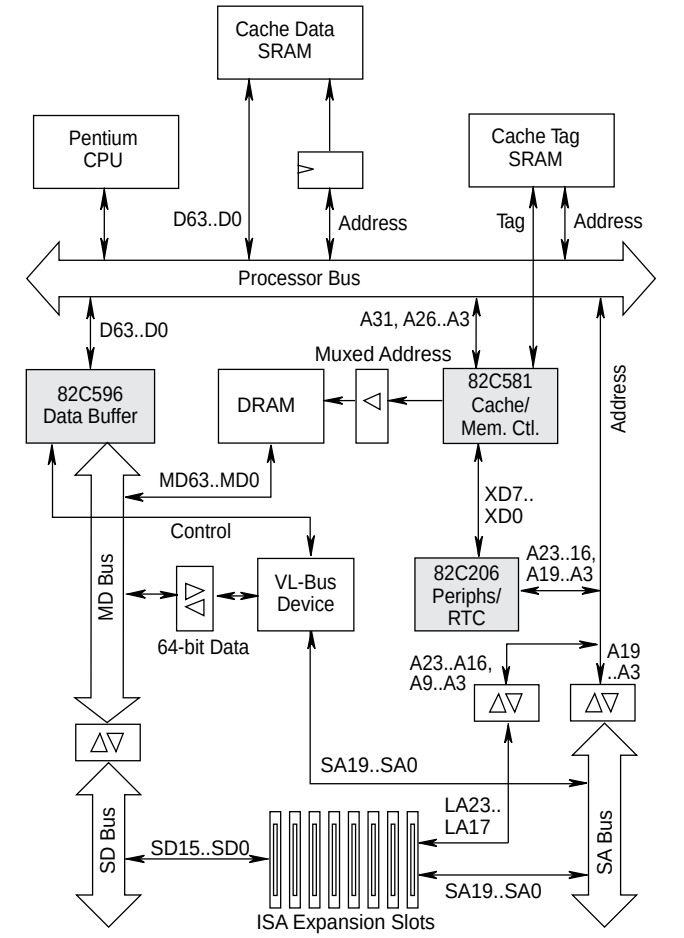

Figure 1. OPTI's chip set converts the Pentium bus to ISA and optionally supports VL-Bus for high-performance peripherals.

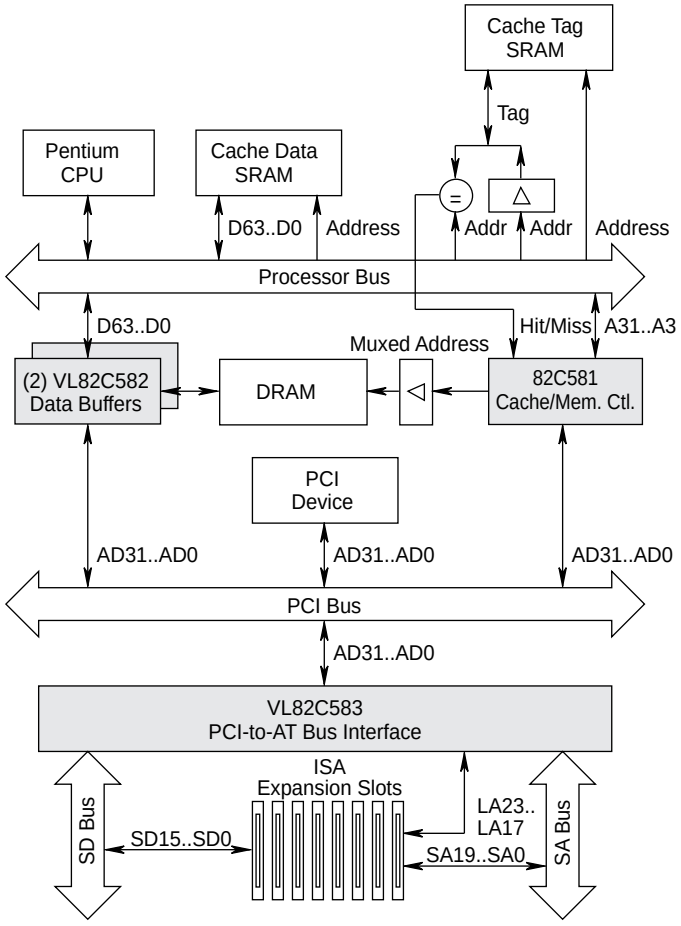

Figure 2. VLSI provides a bridge to PCI, which can then be connected to ISA for standard periperhals.

transfer) using standard SRAMs, or 3-1-1-1 using synchronous SRAMs. Pipelined reads from synchronous SRAMs occur at 1-1-1-1.

The DRAM controller supports read bursts as fast as 6-3-3-3 on page hits using fast 60-ns parts. Slower bursts are available for 70- and 80-ns parts.

OPTi PTMAWB-V Opts for VL-Bus

Figure 1 is a block diagram of OPTi's first Pentium-based chip set. Like the PCI-based designs, the PTMAWB-V chip set supports cache and a local bus. The 82C596 handles system control for the CPU/cache/DRAM section of the board, and contains the ISA bus controller. The 82C597 handles data buffering and conversion between 64-bit host cycles and 32-bit VL-Bus cycles. An 82C206 provides the standard AT peripherals and a real-time clock.

The VL-Bus is a close superset of the signals on the pins of the 486, and is easily synthesized from the processor bus. Many vendors that claim VL-Bus support merely offer an LDEV# (local device address select) signal, to allow external logic to indicate when a local bus device is the target of a bus cycle. (Normally, undecoded cycles default to the expansion bus.)

OPTi goes further by providing a separate VL-Bus controller in the VL82C597, so that local bus cycles can occur independently of cycles on the processor bus. One VL-Bus master and one slave can be supported without adding glue logic.

OPTi's direct-mapped cache controller uses a technique they call "adaptive write-back" (AWB) in which the cache is write-through on a cycle that would be a DRAM page hit or write-back if the cycle is a page miss. The cache can also be operated in normal write-through or write-back modes. The cache tag comparator is on-chip; external tag SRAMs are required. The cache controller supports 3-2-2-2 burst reads using two interleaved banks of standard SRAMs.

At 66 MHz, the DRAM controller supports 8-3-3-3 burst reads on page hits (3-3-3-3 for pipelined transfers) using 70-ns parts. This is a slightly faster total burst time than the 7-4-4-4 pattern achieved by the Intel chip set with similar DRAMs.

VLSI VL82C580 Matches PCIset

Figure 2 is a block diagram of VLSI Technology's VL82C580 chip set. The four-chip design is very similar to Intel's chip set, using one VL82C581 cache/DRAM controller and two VL82C582 data buffer chips. The VL82C583 creates a PCI-to-ISA bus bridge.

Unlike the Intel design, both the tag SRAM and tag comparator are external. Several companies, such as TI and IDT, provide SRAMs with on-chip tag comparators, but there is a price premium for those chips (a small premium, compared to the cost of other components in the high-end systems which would use Pentium and PCI).

The cache controller will support 3-2-2-2 bursts using standard SRAMs and 2-1-1-1 using synchronous SRAMs. Pipelined reads from synchronous SRAMs will occur at 1-1-1-1. The DRAM controller will support bursts as fast as 6-2-2-2 using 60 ns parts at 66 MHz.

The VLSI design appears to have an advantage in maximum memory size, but the 1G size can be achieved only with future 64-Mbit DRAMs. All three designs are roughly equivalent when using current 4-Mbit and 16-Mbit parts.

The 'C580 lists for $65, compared to $84 for Intel's solution, but the cost of the external tag RAM and comparator could quickly eliminate that savings. The VLSI design is also about six months behind Intel's.

Multiprocessor Chip Sets

Pentium processors are likely to be popular for multiprocessor (MP) servers, and with the advent of Windows NT, even single-user desktop systems can use two or more CPUs. An effective shared-memory MP system requires a high-bandwidth bus connecting the processors and memory, and this bus must support cache coherency protocols. PCI isn't up to the challenge, nor is VL-Bus, EISA, or Micro Channel.

Corollary, a pioneer in PC-compatible MP systems, announced plans back in 1991 (see µPR 8/21/91, p. 1) for a multiprocessor chip set for 486 systems. In early 1992, the company redirected the design to a Pentium chip set. Based around its C-bus II multiprocessor bus, the set consists of two chips: the CBC (cache bus controller), and the DPX (data path exchange) chip. The CPU-to-C-bus II interface requires one CBC and two DPX chips. The DPX chips can also be used on memory boards or bridges to external buses, but no integrated memory or expansion bus control logic is provided, making this a less than fully integrated solution. Corollary will provide a complete design kit, however, eliminating the need to design the required logic.

C-bus II has recently been upgraded to 50 MHz using low-voltage-swing GTL transceivers, improving peak bandwidth to 400 Mbytes per second. Corollary also added support for Intel's APIC interrupt controller. The Pentium MP chip set is expected to sample in 3Q93.

LSI Logic is developing a fully integrated chip set for MP Pentium systems. The unannounced "Hydra" design, shown in Figure 3, uses just one chip per processor plus three more for the memory and PCI interfaces. Cache coherency is maintained across the MPI bus, a 33-MHz, multiplexed address/data bus with a peak bandwidth of 233 Mbytes/s. Both MPI and C-bus II use block transfers for memory accesses and support split transactions for I/O accesses.

LSI's design supports a two-way associative cache of up to 1M. Using 11-ns synchronous SRAMs, accesses use a 2-1-1-1 pattern. Unlike Corollary, LSI has integrated dual-ported cache tags on the CCU, eliminating expensive external tag RAMs.

With its high degree of integration, the LSI chip set will undoubtably be less expensive and easier to use than the Corollary design. The bandwidth of the MPI bus

Price and Availability

The price and availability of uniprocessor chip sets are indicated in Table 1. For more information, contact:

Intel, P.O. Box 58119, Santa Clara, CA 95052-8119; 408/765-8080, fax 916/351-5033.

OPTi, 2525 Walsh Avenue, Santa Clara, CA 95051; 408/980-8178, fax 408/980-8860.

VLSI Technology, 8375 South River Parkway, Tempe, AZ 85284; 602/752-8574; fax 602/752-6000.

The Corollary and LSI designs are not announced. For more information, contact:

Corollary, PO Box 18977, Irvine, CA 92713; 714/250-4040, fax 714/250-4043. Ask for George White.

LSI Logic, Headland Division, 1110-401 The West Mall, Etobicoke, Ontario, Canada M9C 5J5; 416/620-7400, fax 416/620-5005. Ask for Philip Eisler.

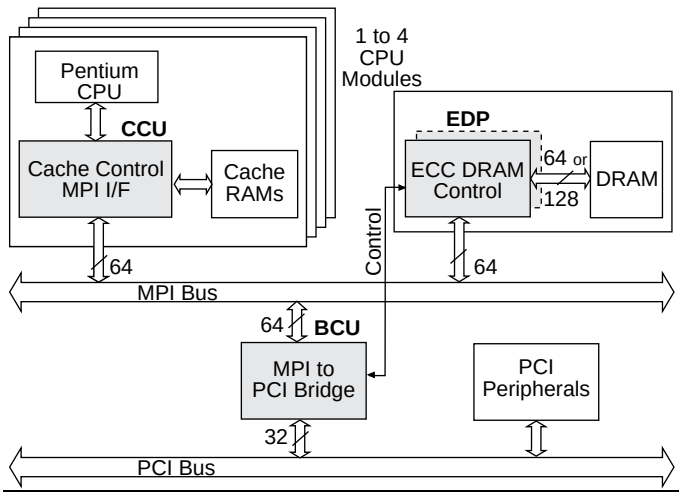

Figure 3. LSI's "Hydra" chip set supports up to four processors using its proprietary high-bandwidth MPI bus.

should be sufficient for systems with 2–4 Pentium processors; the higher-bandwidth C-bus II may be more attractive for high-end servers. LSI plans to begin sampling its chip set in 4Q93.

Conclusions

All three uniprocessor chip sets offer high-end solutions for feature-laden system board designs. Intel has the advantage of offering more modularity, using the PCI bus as a common interface for its ISA and EISA bus bridge chips. A family of board-level products ranging from 486SX to Pentium and ISA to EISA could be constructed using various combinations of Intel's chip set devices. Also, its Pentium-based chip set integrates the tag RAM and tag comparator, simplifying the design of the high-frequency section of the system board.

OPTi's design provides about the same cache functions as the other designs but for graphics substitutes a VL-Bus instead of PCI. Although VL-Bus is closer to the native processor bus than PCI, the OPTi chip set offers little cost savings over the Intel design. It also lacks on-chip tag memory and support for synchronous SRAMs.

VLSI's chip set lacks both on-chip tag memory and an on-chip tag comparator. When an integrated tag SRAM is used, however, the total system chip count can be quite low because on-chip buffers for the memory buses, PCI bus, and expansion buses virtually eliminate glue logic.

Other vendors will have their turn at the plate, but after the first two batters, Intel is leading in the Pentium chip-set game. The two multiprocessor chip sets will make it easier for vendors to design MP Pentium systems but won't impact the market until next year. The presence of multiple chip set vendors shows support for PCI and will keep pressure on Intel to keep prices low. ♦

