Few µP Developments At 40th ISSCC

Commemorative Supplement Issued In Honor of 40th Anniversary

By Brian Case

The 1993 International Solid State Circuits Conference marks the 40th anniversary of this important integrated circuit technology conference. ISSCC has chronicled just about every significant semiconductor advance, including the invention of integrated circuits just a few years after the conference's founding.

While much in the world of solid-state circuits has changed, ISSCC clings staunchly to its traditions. The proceedings are still printed on thick, glossy paper which makes them surprisingly heavy and almost unwieldy. While somewhat relaxed, the rule that an ISSCC paper must be the first public disclosure of a circuit remains in force. To make the ISSCC program, a chip description must be submitted to the committee six months ahead of the conference date—and silicon must have been fabbed—yet it must be kept otherwise secret.

This makes ISSCC increasingly useless as an announcement vehicle for most major integrated-circuit developments, especially microprocessors. Last year, papers on the first Alpha implementation and SuperSPARC were presented. This year, no microprocessor of commercial significance was described.

256M DRAMs Debut

Perhaps the most interesting papers from the point of view of computers this year described memory chips. Last year, while some SRAM activity was apparent, precious little DRAM development was described. This year, three 256-Mbit DRAMs, two 16-Mbit SRAMs, and an SRAM-intensive gate array were presented.

The three 256-Mbit DRAMs consisted of two traditional chips from Hitachi and NEC and a block-structured memory from Toshiba. The chips from Hitachi and NEC are fabricated in 0.25-µm CMOS, while Toshiba used a 0.4-µm CMOS process. Clearly, memory vendors are continuing to push process technology aggressively.

The Hitachi chip is organized as 64M × 4 and has an access time of 70 ns. The chip can operate on voltages from 1.5 V to 3.6 V, and has an active current dissipation of 34 mA (at 3.6 V and a cycle time of 130 ns). The major innovation of the Hitachi part beyond the density is its redundancy technique: subarray replacement instead of simple column and row replacement. Despite the 0.25-µm process, the chip size is a staggering 14.4 mm × 33.2 mm, or about twice the area of SuperSPARC.

The size of NEC's chip is a little more reasonable—but still huge—at 13.6 mm × 24.5 mm. This memory can be organized as either 16M × 16 or 64M × 4 and achieves a typical access time of 30 ns. The chip can operate from a power supply of between 2.0 V and 3.3 V and consumes 35 mA (at 3.3 V and a 60 ns cycle time). NEC designed this DRAM with a traditional row/column redundancy technique (two rows and two columns per 64 Mbit).

The Toshiba DRAM attempts to reduce chip area by designing a block-oriented memory. Instead of a bit-line connection for every one or two DRAM cells, the Toshiba design has four cells connected serially and only one bit-line connection for the group. While this organization results in a non-traditional serial access mode, it also results in a 37% reduction in average cell area and a 32% reduction in chip area compared to a conventional design. The chip is almost as big as the Hitachi chip, but this is mostly because of the much less dense process (0.4 µm vs 0.25 µm). This block-oriented chip has an organization of 32M × 8, a random access time of 112 ns but a serial cycle time of 30 ns, and a power supply of 3.3 V.

Sony and Hitachi presented the two 16-Mbit SRAMs. The Sony part has an access time of 9 ns at 3.3 V or 21 ns at 2.0 V, with a current consumption of 72 mA at 30 MHz. Process technology is 0.35 µm, four-poly, double-metal resulting in a die size of 9.7 mm × 21.9 mm.

A more dense process—0.25 µm, five-poly, double-metal—makes the Hitachi part much smaller. It has a die size—10.4 mm × 10.6 mm—just over half that of the Sony chip. Hitachi's chip operates from 2.5 V, consumes 40 mA at 20 MHz, and yields an access time of 15 ns.

Both of these SRAMs have 4M × 4 organizations. While this organization and the low-voltage operation are appropriate for portable applications, a wider organization would be better for use in second-level microprocessor caches. For example, a 64-bit wide cache would require 16 of these chips and would result in an extremely large 32 Mbyte cache.

The SRAM-based gate array has a 256-Kbit, 1.5-ns SRAM and an array of 11 K gates with 60 ps unloaded internal gate delay (remember, this is the "room-temperature, typical" conference). The basic gate is an ECL four-input OR/NOR. The chip uses a 0.5 µm, 3.3V BiCMOS technology. The RAM is organized as eight blocks of 1K 32-bit words. Chip size is 11 mm × 11 mm.

DECWRL Presents Hot Chip

The most interesting microprocessor paper was from DECWRL and was a description of the "warm-up" chip for the GHz clock-rate BIPS project *(see **070505.PDF**)*. This

300-MHz ECL chip implements a subset of the R2000 architecture. Worst-case power dissipation at -5.2 V is 115 W, which gave the designers a chance to test their "thermosiphon" cooling tower (wickless heatpipe). The chip is implemented in a 1.0 µm-drawn, one-poly, four-metal process with one layer of gold interconnect for power. The 15.4 mm × 12.6 mm die implements 468,000 transistors.

This chip uses a five-stage pipeline and integrates instruction and data caches of 2K each. There is no FPU or MMU on chip. The plans for the BIPS chip are much more aggressive: much larger caches, on-chip FPU and MMU, and a much denser process.

Intergraph apparently intends to continue using Clipper microprocessors, as it revealed a 32-Kbyte cache memory/MMU chip for the C400 CPU. This chip achieves an impressive 6-ns cycle time. No process details or chip size were given, but the chip uses four-transistor SRAM cells and is claimed to be implemented in a "foundry ASIC process," which makes the fast access time impressive.

A team from the University of Michigan detailed their GaAs microprocessor. Like the DECWRL chip, it implements a subset of the MIPS architecture. The chip is implemented in the Vitesse 1.0 µm (0.6 µm effective) GaAs process and integrates 160,000 transistors on a 13.9 mm × 7.8 mm die. The chip operates on a 2.0 V supply and dissipates 24 W. Unfortunately, the clock rate is low; parts of the chip operate at 200 MHz, but full function has been verified at only 100 MHz due to a clock-phase design error.

Conclusions

The bulk of this year's ISSCC program, as always, covers a wide range of topics including DSP, data conversion, data communications, radio circuits, and other analog circuit topics. It will continue to be the premier conference for technological one-up-manship in those technologies that require years to mature, such as DRAMs and sophisticated analog circuits. For mainstream microprocessors, however, ISSCC fails to attract, a fact that is underscored by the absence from the program of the most significant processor development of 1993—Pentium. The lack of a system focus also makes ISSCC increasingly irrelevant to most of the computer industry.♦

Copies of the ISSCC Digest of Papers can be ordered from John Wuorinen; call him at 207/326-8811.

