68360 Provides Sophisticated Communications

QUICC Is True 32-bit Upgrade For 68302

By Brian Case

The latest member of Motorola's modular 68300 microcontroller family is the impressive 32-bit 68360 QUICC (quad integrated communication controller). The 68360 is a multiprotocol communication engine that offers four high-speed serial ports, three low-speed serial ports, DMA channels, four 16-bit timers, a dedicated communications processor that implements eight different serial protocols, a time-slot assigner for T1 support, and glueless interfaces to DRAM and the 68040.

The full-featured version of the 68360 (using the same die) is the 68EN360, which implements Ethernet support. The 68EN360, together with its companion 68160 enhanced Ethernet serial transceiver, provides a complete Ethernet solution with two chips.

The multiprotocol support of the 68360 will make it especially useful in network end nodes, such as laser printers, that need Ethernet and other communication protocols like AppleTalk and Centronics parallel interface . The popularity of Ethernet in these markets gives the two-chip 68EN630/68160 combination a special advantage. Motorola believes that the chip will also be useful in network bridging and routing applications, but there are probably better solutions.

Although it is philosophically an upgrade of the 16-bit 68302 communications chip, the 68360 is more a true member of the 68300 family because, unlike the 68302, it uses the intermodule bus (IMB) to connect the CPU and on-chip modules; it also replaces the simple 68000 core with the CPU32+. The 68360 is the first implementation to use a 32-bit IMB (previous IMBs were 16-bit).

As shown in Figure 1, the 68360 has the same basic organization as the 68302—a CISC processor core, a system integration module (SIM60), and a communications processor module (CPM)—but the 68360 is much more highly integrated and dramatically improves on the performance of the 68302.

The 68360 uses a static design that initially will allow clock rates of 0–25 MHz. A 33-MHz version is planned. Both the CISC and the controller in the CPM have a "slow-go" mode that allows the main clock to be divided down to reduce power consumption. For example, the CISC clock can be divided by 2, 4, 8, 16, or 32. Slow-go mode does not affect the clocks to the baud-rate generators, however. The 68360 will be available in both 241-pin PGA and 240-pin QFP packages.

CPU32+ Core Provides Control

While the 68302 uses a 68000 processor core, the other 68300-family members are built around a core called the CPU32, which is a slimmed-down 68020 that eliminates the barrel shifter and instruction cache. It also has two new instructions: low-power-stop for power management and table-lookup-and-interpolate for engine control. The 68360's CPU32+ core implements the same instruction set as the CPU32, but it has a full 32-bit interface to the IMB (in contrast to the 16-bit interface of the CPU32) and implements automatic byte alignment, which allows 16- and 32-bit data to be accessed at odd addresses.

SIM60 Integrates System Functions

The system integration module (SIM) on the 68360 (SIM60) is an upgraded version of the SIM40 from the 68340 and 68330 chips. The memory controller has been significantly enhanced to provide a glueless interface for up to eight banks of memory including DRAM, SRAM, EPROM, and EEPROM. DRAM control is now completely glueless for small arrays (e.g., one 16- or 32-bit SIMM) and requires only address buffers for larger arrays.

Another feature of the external interface is "68040 companion mode." With the internal CPU32+ disabled, 68040 companion mode provides a completely glueless interface to an external 68040, as shown in Figure 2. The

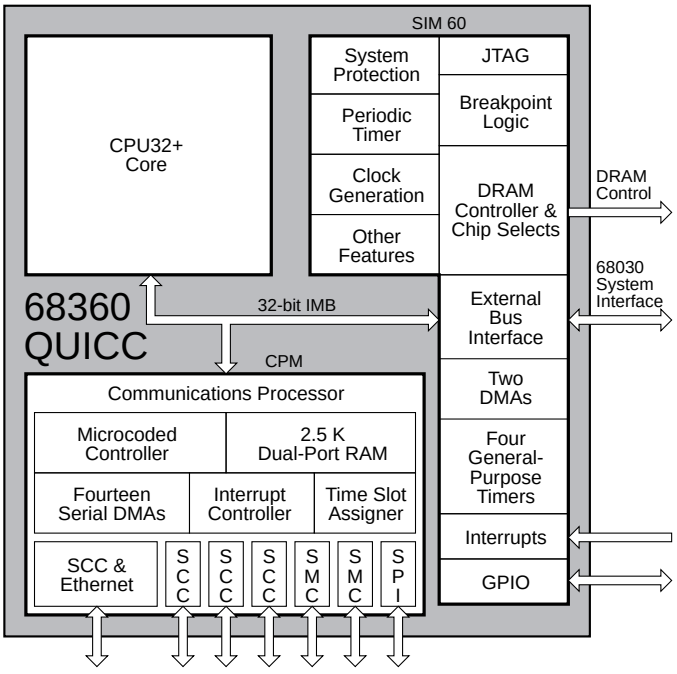


Figure 1. 68EN360 functional block diagram. On the vanilla 68360, the first SCC does not have Ethernet capability.

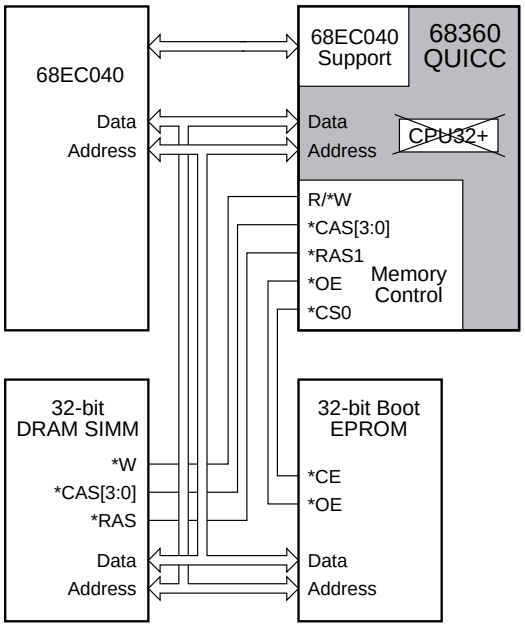


Figure 2. 68040 "companion mode." The internal CPU32+ core is disabled, and the 68040 interfaces directly to the 68360 or 68EN360. As shown, the 68040 can take advantage of the memory control functions, but sacrifices the dynamic bus-sizing capabilities since the data bus does not pass through the 68360.

68040 can transparently access all of the 68360's on-chip functions and make use of the memory controller. The cost-reduced 68EC040 (MMU and FPU eliminated) should be a good match to the 68360 in applications that require more performance than the CPU32+ can deliver. In addition, Motorola says some customers are interested in using the PowerPC 601 with the 68360 in companion mode. The similarities between the 601 and 68040 buses make this feasible.

The external interface, aside from the signals for the memory interface, is a 68030 bus. It is a full 32 bits wide and implements the standard 68020/68030 dynamic bus sizing to gracefully deal with narrower memories. Unfortunately, the dynamic bus sizing is sacrificed in companion mode. A separate chip, the 68150, can be used to provide this feature.

The SIM60 provides a wealth of other miscellaneous system functions. Testing is facilitated through JTAG boundary scan and an on-chip hardware breakpoint. The breakpoint has an address and a mask that allows the break to be qualified by access type, access size, and address space.

Two independent, general-purpose 32-bit DMA channels are available. They offer buffer chaining to reduce CPU overhead and have independent request and acknowledge logic.

The four general-purpose timer/counters on the 68360 are a functional superset of the two 16-bit timers on the 68302, and they can be cascaded to provide 32-bit resolution if required. A separate periodic interval timer is available for simple watchdog functions.

The clock generator can synthesize a full-speed clock signal from a cheap watch crystal to reduce cost. In addition, the low-power standby mode will be useful in applications powered by batteries or phone-line current.

CPM Supports Many Protocols

The autonomous communications processor module (CPM) is the heart of the 68360. It contains a dedicated, microcoded processor (which Motorola calls a RISC) to implement the communication protocols, four high-bandwidth and three low-bandwidth serial ports, 2.5 Kbytes of dual-port RAM, a TDM time-slot assigner, four baud-rate generators, and fourteen DMA channels to support the serial ports.

The processor in the CPM has hardwired microcode for eight protocols: HDLC/SDLC, HDLC Bus (HDLC-based LAN), LocalTalk, Signaling System #7 (a telephone switching-system protocol), UART/USART, Bisync, transparent bit stream, and Ethernet on the 68EN360. The transparent mode can be either totally transparent or frame-based with CRC information appended. In contrast, the 68302 provided only five protocols.

Beyond the built-in protocols, additional protocols can be implemented by downloading microcode into the RAM. So far, Motorola has plans to support five protocols with RAM-based microcode: Profibus (a UART-based industrial control bus), asynchronous HDLC (to support the point-to-point protocol), DDCMP (used in early DECNET implementations), V.14 (a synchronous rate-adaption protocol), and X.21 (a protocol with in-band control signaling).

Optional protocols for the 68302 were also implemented by downloading microcode, but the 68360 provides more RAM and better support. Motorola has already implemented Profibus and DDCMP for the 68302, so these just need to be ported to the 68360. Note that no development tools are available to customers; Motorola must write the microcode for optional protocols.

Part of the dual-port RAM (768 bytes) is used as a memory-mapped register bank. These registers allow the CPU to program the serial channels and the SIM60 functions. The remaining 1792 bytes of RAM are used for local data storage, data buffers for the serial ports, and microcode storage.

The four high-bandwidth serial communication channels (SCC) can be independently programmed to use any available protocol. Each SCC can support a data rate up to 2.048 Mbps (assuming the 68360 is running with a 25-MHz master clock). This is sufficient for both American T1 and European CEPT transmission. American T1 requires 1.544 Mbps to multiplex 24 channels, while European T1 requires 2.048 Mbps for 32 channels.

The other three serial ports are a little less capable. The two serial management controllers (SMC) are intend-

ed to perform framing and serial interface tasks in ISDN-type applications. The SMCs can implement UART, transparent, and GCI (general-circuit interface) protocols. The remaining serial port, the SPI (serial peripheral interface), is intended for communication with other system components such as voice codecs, another microcontroller, or a debugging system.

The 68360 provides four baud-rate generators to determine the data rates of the SCCs and SMCs. The generators are all independent and each can be connected to any SCC or SMC. Speed changes are allowed during operation, and automatic baud rate operation is supported. Autobaud is available for all four SCCs and is enabled by a bit in each baud-rate generator.

In addition to the two general-purpose DMA channels in the SIM60, the CPM has fourteen DMA channels dedicated to the serial ports. These DMA channels can interrupt the CPU32+ through the interrupt controller. Even though each serial port has two DMA channels, only one interrupt vector is assigned to each port.

If desired, some of the pins dedicated to the serial interfaces can be used instead as a parallel port. Up to 46 bits of parallel I/O can be implemented at the expense of all serial ports. If all serial ports are used and all option pins on all ports are enabled, only eight parallel I/O pins remain available.

The interrupt controller is flexible. It prioritizes seven external IRQ lines, 12 parallel-port pins that can be programmed to act as interrupt sources, and 16 internal interrupt sources. The priority among the SCC DMAs is programmable.

To support the time-division multiplexing (TDM) required for T1 and CEPT, the 68360 has a dedicated time-slot assigner that allows the 68360 to mix data from the SCCs and SMCs onto a TDM channel and can work with either bit- or byte-sized data. Up to two TDM channels can be supported simultaneously, and each TDM channel can use one of several protocols: T1, CEPT, PCM highway, ISDN basic rate (aggregate throughput of 144 kbps), ISDN primary rate (aggregate throughput of 2.048 Mbps), or user defined.

Built-In Ethernet Support

The 68EN360 is a fully functional, higher-cost version of the 68360 that supports the 10-Mbps Ethernet data rate on the first SCC. It implements the entire media access control layer of the IEEE 802.3 Ethernet standard, but requires an external serial interface adapter and Ethernet transceiver.

The 68160 enhanced Ethernet serial transceiver from Motorola provides these functions with a glueless interface to the 68EN360. The 68160 can interface to both 10BASE-T twisted-pair cable and coaxial cable. Motorola implemented the 68160 in BiCMOS to provide the bipolar drivers required for these interfaces. The 68160 is packaged in a 52-pin surface-mount thin QFP.

Price & Availability

Samples of the 68360 are available now in a 240-pin QFP. Production pricing will be $50 in quantities of 10,000. The 68EN360 will sample in September, with production pricing at $60 in quantities of 10,000. Full production for both parts is expected to begin in the fourth quarter.

Production quantities of the 68160 Ethernet adapter will be available in September in a 52-pin QFP. The price will be $10 in quantities of 10,000.

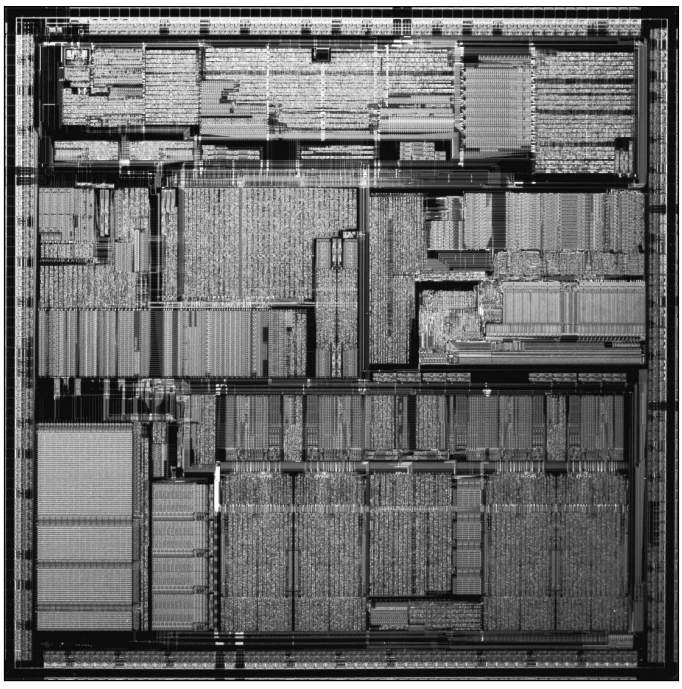
The QUADS development system is available now for $1995.

Contact Trey Oprendek at Motorola, MS OE216, 6501 William Cannon Drive West, Austin TX, 78735; 512/891-3434, fax 512/891-2143.

Development Support Available

Motorola offers its own QUADS evaluation board with two 68360s, a 68160, 512K of EPROM, 1M of DRAM, and several serial connectors including Ethernet and LocalTalk. Through a package adapter, the QUADS board can emulate a 68360 for target system debugging. The board can be controlled by either a dumb terminal or a host computer, which can be an IBM PC or a Sun workstation. The QUADS board also connects directly to a logic analyzer.

The 68360 is well supported by third-party vendors. Hardware in-circuit emulators are planned by Applied



Die Photo of QUICC. The chip uses 750,000 transistors; Motorola refused to give the die size or identify the functional blocks.

Microsystems, HP, and Huntsville Microsystems. Software development support will be available from Intermetrics, Microtec Research, Software Development Systems, Ready Systems, and Embedded Support Tools (EST). Embedded protocol and microkernel OS support is promised from Integrated Systems, Wind River Systems, MetaSphere, and Pacific Softworks.

Conclusions

Motorola believes the 68360 will be useful in bridges and routers, but these applications will probably require the use of a 68040 in companion mode because full wire-speed Ethernet alone requires about 15 MIPS of processor performance to achieve the peak rate of 15,000 packets per second. Since a separate processor is required anyway, there are other single-chip Ethernet solutions (from National, for example) that don't use a processor and would result in an equally good (or better) system design.

The 68360 does, however, look good for end-node applications such as line cards in telephone and PBX switches and multiprotocol controllers in personal computers and peripherals.

The 68360 sets a new standard for high integration in communication controllers, and the 68EN360 goes even further as the first microprocessor to integrate an Ethernet controller. The 68360 illustrates the fact that the trend toward higher integration in embedded controllers results in chips that are increasingly application specific. Application specificity allows the integration of a large number of functions, which in turn allows semiconductor manufacturers to take advantage of the high transistor counts now available.

So far, the most visible design win for embedded RISCs has been as controllers for laser printers, but the communications market is likely to be the next big, visible opportunity for embedded control. The 68360 is a good example of how Motorola can compete effectively with the successful, mainstream RISCs by integrating a dedicated controller, peripheral functions, and a general-purpose CISC. By exploiting its strengths—expertise in communication protocols and the modular structure of the 68300 family—Motorola has carved out a defensible product niche. ♦

