Motorola Introduces Another 8-Bit µC Family

68HC08 Plugs Small Gap Between '05 and '11

By Mark Thorson

Positioned precisely between the popular 68HC05 and 68HC11 families—and not intended as a replacement for either one—the 68HC08 is a faster and architecturally-enhanced version of Motorola's low-end 8-bit processor line, the 68HC05. It extends the instruction set and architecture, mostly in the area of supporting an overflow flag (the V bit), 16-bit address registers (index, stack pointer, and PC), and new stack-pointer-relative addressing modes. It is intended for low-end 8-bit applications that push the limits of the venerable 68HC05 but cannot afford the more expensive 68HC11 (see µPR 10/17/90, p. 9).

Motorola is using a 0.8-micron process and a new generation of CAD tools, the latter expected to help produce new designs at an even greater rate than the already feverish pace Motorola has demonstrated in generating new versions of the '05 (see sidebar, page 19). Internally, the '08 has a strictly defined bus which, in combination with a developing library of constant-height (i.e., identical in one dimension) peripheral cells, Motorola expects to allow a much shorter turnaround time to design parts for highly specialized applications, similar to the versatility shown with the 68300 family. An on-chip coprocessor protocol provides efficient support for the DMA controller. Hardware support for DSP and fuzzy logic are planned.

Performance has been improved over the '05 through both doubling the clock speed (to 8 MHz) and reducing the clock cycles per instruction by about one cycle out of three or four for a typical instruction.

A Highly Integrated Microcontroller

Figure 1 is a block diagram of the first member of the family, which will be available in both ROM and EPROM versions (the 68HC08XL36 and 68HC708XL36, respectively). The core processor can be thought of as an extended 68HC05 CPU, although the ALU still handles 8 bits at a time. The CPU connects to the other modules on the chip via the internal bus (IBUS), which also supports bus masters and future coprocessors, the latter using special instructions for fast register load and bus protocols that allow visibility into the CPU registers. These coprocessors are not included in the 'XL36, the first component in the '08 family.

The new chip has a bus-master DMA unit that handles transfers at up to 4 Mbytes/s. The current version uses only the bus-master capabilities of IBUS, but future plans call for parts with DSP and fuzzy logic hardware that are more coprocessor-like.

The 'XL36 contains 1 Kbyte of RAM and 36 Kbytes of ROM or EPROM. There are no provisions for adding external memory; the internal bus, true to its name, does not go off of the chip. It is also difficult to add I/O devices beyond those included in the chip.

The new chip has a 16-bit counter/timer, with a programmable prescaler, that drives four sets of compare registers. This is useful for generating precisely timed signals, such as pulse-width modulation (PWM) outputs.

The clock-generation module provides an on-chip phase-locked loop (PLL) to generate the CPU clock from an external 1-MHz crystal. Future parts will support 32-kHz watch crystals.

The system integration module handles reset, bus control, interrupts, a watchdog timer, and low-voltage

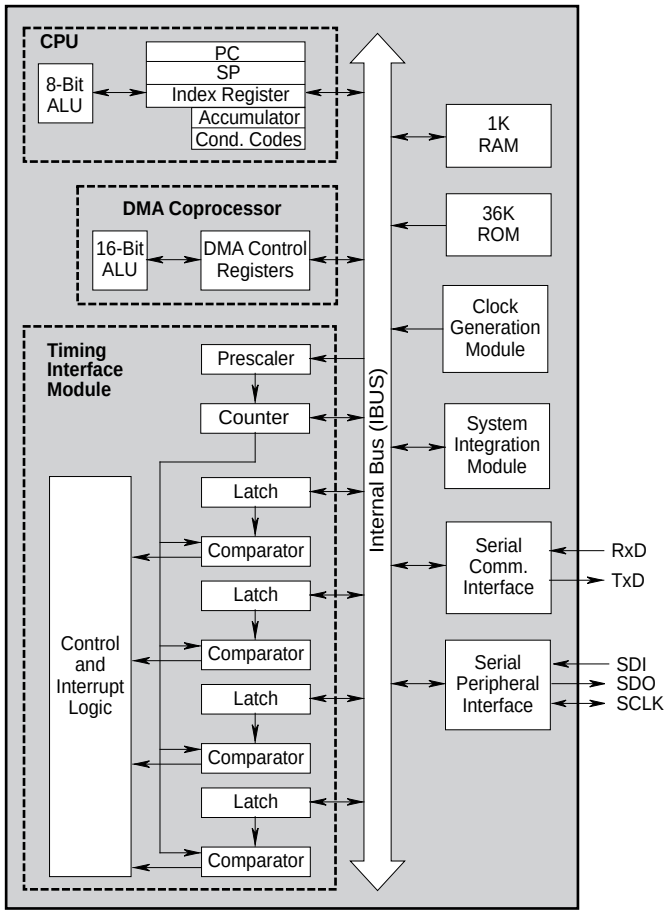

Figure 1. The 68HC08XL36 is a complete 8-bit microcontroller with up to 36K of internal ROM or EPROM.

Mnemonic	Instruction
AIS	Add 8-bit signed immediate to 16-bit stack pointer
AIX	Add 8-bit signed immediate to 16-bit HX register
BGE	Branch if greater than or equal
BGT	Branch if greater than
BLE	Branch if less than or equal
BLT	Branch if less than
CBEQ	Compare operand to accumulator and branch if equal
CBEQA	Compare immediate to accumulator and branch if equal
CBEQX	Compare X register (low byte of index register) to accumulator and branch if equal
CLRH	Clear H register (high byte of index register)
CPHX	Compare 16-bit immediate or 16-bit direct-addressed operand with HX register
DAA	Decimal adjust accumulator
DBNZ	Decrement operand and branch if not zero
DBNZA	Decrement accumulator and branch if not zero
DBNZX	Decrement X register (low byte of index register) and branch if not zero
DIV	Divide
LDHX	Load 16-bit immediate or 16-bit direct-addressed operand into HX register
MOV	Memory-to-memory move (see text)
NSA	Nibble swap accumulator
PSHA	Push accumulator onto stack
PSHH	Push H register (high byte of index register) onto stack
PSHX	Push X register (low byte of index register) onto stack
PULA	Pop the stack into the accumulator
PULH	Pop the stack into the H register (high byte of index register)
PULX	Pop the stack into the X register (low byte of index register)
STHX	Store HX register to 16-bit direct-addressed operand
TAP	Transfer accumulator to condition code register
TPA	Transfer condition code register to accumulator
TSX	Transfer 16-bit stack pointer plus one to the HX register
TXS	Transfer 16-bit HX register minus one to the stack pointer

Table 1. The 68HC08 family extends the 68HC05 instruction set with the new instructions shown here.

sensing. The watchdog timer and low-voltage circuits can reset the chip. Illegal opcodes or addresses also cause a reset, which is useful in noisy environments if processor registers or memory become corrupted.

The ’XL36 has a UART (up to 76.8 kbaud) and a clocked serial interface (up to 1 Mbaud). The latter is useful for common three-wire buses such as Philips’ I²C bus used for interface to serial EEPROMs, LCD display controllers, and similar devices.

Instruction Set and Register File

The instruction set can be classified as accumulator-oriented, because all double-operand arithmetic and logical instructions require the accumulator to be the destination operand. Table 1 shows the new instructions introduced in the 68HC08 instruction set. The instruction set is a strict superset of the 68HC05.

Prominent among the new instructions are a divide instruction and a set of memory-to-memory move instructions. A modicum of 8-bit by 16-bit arithmetic is provided, and the new data-transfer instructions make the X register almost as useful as a second accumulator.

The addressing modes are upward-compatible from the 68HC05, with only the length of the program counter, index register, and stack pointer increasing, as shown in Figure 2.

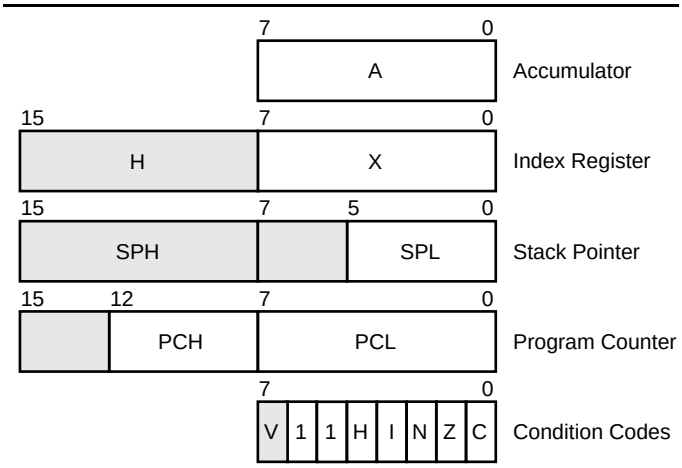

Figure 2. The 68HC08 extends some of the 68HC05 registers to 16 bits, as indicated by the shaded portions of the figure.

The 68HC08 supports the 68HC05 addressing modes for the source operand of double-operand arithmetic and logical instructions (except MUL and DIV), including immediate, direct, extended indexed (no offset), and indexed (8- or 16-bit offset). In addition, it supports two new modes:

- Stack Pointer (8-bit offset)—the operand address is the unsigned sum of an 8-bit offset and the stack pointer.
- Stack Pointer (16-bit offset)—the operand address is the unsigned sum of a 16-bit offset and the stack pointer.

The destination operand of single-operand arithmetic and logical instructions is more limited, with only one new addressing mode (stack pointer with 8-bit offset).

There are also special modes available only for the MOV (memory-to-memory transfer) instruction:

- Immediate-to-Direct—loads an 8-bit immediate into one of the first 256 bytes of memory.
- Direct-to-Direct—transfers one byte to another, both within the first 256 bytes of memory.
- Indexed-Postincrement-to-Direct—transfers a byte addressed by the 16-bit index register to a direct location, then increments the index register.
- Direct-to-Indexed-Postincrement—transfers a byte from a direct location to the byte addressed by the 16-bit index register, then increments the index register.

These modes did not exist on the ’05, and they greatly relieve the accumulator bottleneck.

Branches are supported for all useful combinations of the condition codes. The ’08 contains a new flag, the V bit, which indicates that the previous arithmetic result had an overflow (assuming two’s-complement arithmetic). A CISC-like compare-and-branch-if-equal instruction is included for rapid table and string searching.

The time to perform an 8-bit by 8-bit unsigned

68HC05 Still Going Strong

In announcing the 68HC08 family, Motorola stresses that it is not replacing the venerable 68HC05 family. The '08 offers a performance growth path designed to resist competitive pressure, such as the recent devices from Microchip. Motorola will continue to introduce new devices in the already enormous '05 family. Unless an application needs the higher performance or better addressing capabilities of the '08, it will probably stay with the '05 because of price.

Introduced in 1984, the 'HC05 architecture is like a cut-down 6800 architecture, lacking the second accumulator, index register, and several bits from the program counter and stack pointer.

Today, both the older NMOS 6805 family and the more recent CMOS 68HC05 are available in volume in a wide array of configurations. There are 53 standard 68HC05 ROM-based parts, 25 EPROM or EEPROM parts, and one ROM-less part. In the 6805 portfolio, there are nine ROM parts and four EPROM parts.

Memory sizes in the 68HC05 family range from 0.5 to 32 Kbytes of ROM and 32 to 1024 bytes of RAM. There is a huge variety of peripherals. In addition to UARTs, clocked serial I/O, timers, and general-purpose outputs, there are application-specific peripherals such as TV on-screen character generators, LCD display drivers, and tone generators for telephones. A few devices have on-chip EEPROM, in sizes from 32 bytes to 6 Kbytes.

multiply with a 16-bit product has been reduced from 2750 ns ('05 at 4 MHz) to 625 ns ('08 at 8 MHz). The source operands are taken from the 8-bit X and A registers, and a 16-bit result is left in the 16-bit concatenated XA register. The '08 introduces a 16-bit by 8-bit unsigned divide instruction (the '05 has no divide) that produces an 8-bit quotient and remainder in the A and H registers from a 16-bit dividend in HA and an 8-bit divisor in the X register. It requires 875 ns at 8 MHz.

Two power-down modes are available through the WAIT and STOP instructions. WAIT suspends the clock to the CPU, leaving the on-chip peripherals (including the timer) running. Any interrupt breaks out of this mode. STOP shuts down the peripherals, including the timer and the oscillator clock; only an external interrupt or reset can break out of this mode. No specifications are currently available for power consumption in active or idle modes.

Development Tools

Hardware and software development tools are planned for availability in the fourth quarter of this year. IASM08 is an editor, assembler, and debugger for PC-compatible systems. SMUL8 is a software simulator. IASM08 and SMUL8 are available now free of charge. Requests for the software should be faxed to Motorola at 800/347-6686.

Price & Availability

The 68HC08XL36 will cost $6.50 in 10,000-unit quantity, in a 56-pin shrink DIP or 64-lead PQFP. The EPROM version (68HC708XL36) will cost $30 in 100-unit quantity. Samples of the 68HC708XL36 will be available in 4Q93. Production quantities of both chips will be available in 2H94.

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ICS08 is a low-cost non-real-time emulator board, while EVS08 is similar to Motorola's boards for the '05 and '11 families, supporting real-time emulation. The Motorola Modular Development System (MMDS08) is a full-featured high-end development system with device-specific in-circuit emulation pods, and bus state analyzer. No pricing is yet available, but it will be comparable to similar development tools for the '05.

Third-party support for the C language is planned by Byte Craft Ltd. (Waterloo, Ontario).

Conclusion

The 6805 architecture was originally designed for minimum cost to serve low-end applications, competing against 4-bit architectures like TI's TMS1000 and National Semiconductor's COPS family, and low-end 8-bit architectures such as Microchip's (then General Instruments) PIC family. Time and competitive pressure have forced a revamping of this architecture, at least to the extent of filling in the most obvious holes.

The condition codes now include the complete set of ZNCV bits, the address registers have been extended to 16 bits, and the accumulator bottleneck has been relaxed by the introduction of instructions that make the index register more accessible. These features, combined with aggressive pricing, will make it a fierce competitor for mainstream 8-bit microcontroller architectures, such as the 8051 and its derivatives.

The 68HC08 architecture will not make an immediate impact, as the first parts are not expected to sample until the fourth quarter, with production in the middle of next year. It does, however, remedy the major deficiencies in the '05 design without providing a platform for migrating applications from the 68HC11, allowing Motorola to maintain this pricier product line. (It would not be difficult to port an assembly-level application from the '05 to the '11 because the architecture is nearly a proper superset, but porting in the reverse direction would be difficult.) Motorola's commanding position as a microcontroller supplier ensures that the 68HC08 will be an important family in the low-end to mid-range market for many years to come. ♦

