LSI Delivers MPEG Decoder for Digital TV

With 720 × 480 Resolution, L64112 is Precursor to MPEG-2 Chip

By Linley Gwennap

LSI Logic has announced an MPEG decoder chip with broadcast-TV quality, challenging C-Cube's dominance in this area. Delivering four times the resolution of typical MPEG-1 parts, the L64112 accepts data at up to 15 Mbps. It is the first generally available chip to provide CCIR601 resolution (720 × 480 at 30 Hz) in real time. The company designed the new part for emerging video applications such as digital cable TV, interactive TV, digital VCRs, and laser disc players. It can also be used to create high-quality images in multimedia PCs.

Complete MPEG System Design

Figure 1 shows the 64112 in a typical system. The video chip takes its data from either a serial stream (in a broadcast application) or an 8-bit parallel bus (from a storage device or in a PC). The chip extracts video frames from the MPEG data stream and performs the required Huffman decoding, inverse discrete cosine transformation (IDCT), motion compensation, and pixel interpolation *(see **060803.PDF** for a description of the MPEG algorithm)*. The chip operates at 27 MHz to reach its maximum resolution and frame rate.

Since an MPEG decoder must be able to interpolate pixels from two different frames at once, it needs sufficient memory to store at least two complete frames. The 64112 includes a glueless interface to external DRAM for this purpose. Four×16 parts are typically used for the 64-bit interface. CCIR applications require 2 Mbytes of memory (four 4-Mbit parts), but 512 Kbytes can be substituted for less demanding CIF resolution (352 × 288).

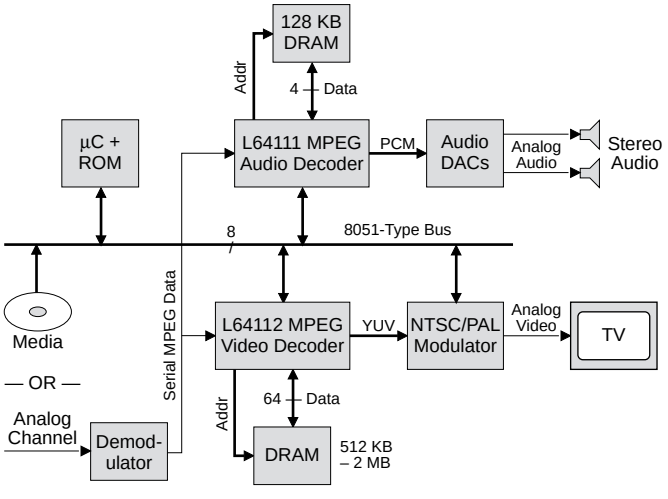

Figure 1. A typical application takes MPEG data either from an 8-bit storage device or as a serial stream from a demodulated channel, providing stereo sound and TV-quality video.

The 64112 outputs the decoded images in YUV (luminance and chrominance) format using a bus width of 8, 16, or 24 bits. A standard NTSC or PAL modulator converts this data to an analog format suitable for American or British televisions, respectively. When used in a PC, the video chip produces progressive (non-interlaced) output, but it requires external logic to convert from YUV to RGB format for a standard monitor. In this case, a RAMDAC replaces the modulator.

A companion chip, the 64111, decodes the audio portion of the MPEG data stream. It is externally similar to the 64112 except that it sends digital audio data to a pair of audio DACs that drive stereo speakers. Because the memory requirements for audio are less than for video, the audio chip uses only 128 Kbytes of external DRAM for a buffer, as shown in Figure 1.

A microcontroller connects to the 8-bit parallel port of both the video and audio chips. It plays no role in the MPEG decoding process but performs initialization and test functions. It can set up the video chip in a variety of configurations, selecting such parameters as frame size, frame rate, synchronization pulse width, error concealment mode, and 3:2 pulldown mode (for converting from 24 to 30 frames per second). During normal operation, the microcontroller monitors status and can reprogram video parameters on the fly. For simple applications, an 8051-type CPU can be used to control the system.

Microcode Engine Performs Decoding

Internally, the 64112 is a specialized microcode engine, as shown in Figure 2. A semi-autonomous preprocessor extracts the video frames from the MPEG data stream and then the microcode goes to work. The onboard controller tells the various functional units what to do. These units are designed to efficiently perform the calculations required by the MPEG algorithm. Completed pixels are delivered to the display unit, which does the final YUV encoding and sends them to the modulator.

All microcode is stored in an on-chip ROM. This eliminates the need for external code storage but prevents the chip from being easily reprogrammed for other algorithms. LSI would not reveal the width or size of the microcode store.

Although LSI has a MIPS processor core in-house, it decided instead to design a custom microcode engine for its MPEG decoder. The company believes that a spe-

cialized controller helps it meet the high-performance and low-cost objectives for its chip.

This tactic contrasts with the direction taken by IIT and C-Cube, which use RISC cores to control their video decoder chips. IIT licensed the MIPS-X core from Stanford (see µPR 10/30/91, p. 1) while C-Cube designed its own RISC controller with 32-bit, single-cycle instructions *(see **060803.PDF**)*. For LSI, using its MIPS core would have saved some design effort, but the final design would have been too large and expensive. Instead of removing the unneeded features from the MIPS core, LSI felt it was easier to start from scratch.

First with Inexpensive TV Quality

The first wave of low-cost video chips implemented the MPEG-1 standard, which specifies CIF resolution at a data rate of 1.2 Mbps. These specifications match the capabilities of CD-ROMs or hard disks, allowing these chips to be used in multimedia PCs, video games, and interactive-television products.

While CIF resolution is adequate for displaying video in a small window on a PC monitor, these images must be expanded by pixel duplication for a full-size television screen. On a typical TV, CIF images appear blocky and slightly distorted, but this lower quality has been accepted because of the difficulty of both encoding and transmitting denser images.

MPEG-1 products include C-Cube's CL450 MPEG decoder and SGS-Thomson's STi3240 video decoder. Both of these products sell for about $50. LSI lists its decoder at $125 for samples but says that pricing in consumer-product quantities could be "less than half" of this amount. The company believes that it is charging only a small premium for higher-quality images.

C-Cube's CL950 is the only other chip that offers CCIR resolution, but it is not sold on the open market. The '950 is generally thought to be more expensive than LSI's device.

LSI's 64112 is most appropriate for applications that require full CCIR resolution for broadcast-TV quality. It is not as well-suited for CD-ROM video or other CIF applications because of its cost premium. It can be used in multimedia PCs, but again only for applications that require high-quality full-screen images; the lower-priced CIF chips are more cost-effective when video-in-a-window is acceptable.

Ready for MPEG-2

The MPEG-2 specification has only recently been frozen and has not yet been ratified. Thus, no vendors have yet offered a fully-compliant MPEG-2 chip. Because MPEG-2 requires high-resolution 720 × 480 images and data rates up to 15 Mbps, LSI has a head-start over other vendors by incorporating these features into the 64112. The company also believes that the chip's internal processing capabilities and memory bandwidth are adequate for MPEG-2.

Since the LSI design, unlike C-Cube's, includes its programming in on-chip ROM, the current release of the chip will not be upgradeable to MPEG-2 in the field. LSI has already begun to develop MPEG-2 microcode for the 64112 and expects to be the first company to deliver an decoder for MPEG-2.

Competition Will Intensify

As the MPEG-2 standard solidifies, other vendors plan to offer chips with similar capabilities as the 64112. Both IIT and SGS-Thomson expect to deliver chip sets in 2H93 that encode and decode MPEG-2. C-Cube and AT&T will probably also enter this market. LSI is developing an encoder chip that will allow it to build a complete codec similar to other chip sets.

LSI has gained a head start in the MPEG-2 race by leaping into the market with a partial solution before the standard is finalized. The company has already gained design wins at CD-pioneer Philips to develop chips for digital televisions. Once other companies challenge LSI with their own TV-quality chips, prices will drop and new market leaders may emerge. ♦

Price and Availability

The L64112 video decoder, which uses a 208-pin MQUAD package, is currently sampling at $125 each. LSI expects to begin volume shipments in June. The L64111 audio decoder is currently in production using a 100-pin PQFP package. Pricing is $36 in sample quantities. LSI did not disclose volume pricing for these chips but says it is up to 50% lower for large volumes.

For more information, contact LSI Logic's Literature Distribution Center, MS D-102, 1551 McCarthy Blvd., Milpitas, CA 95035; 408/433-8000.

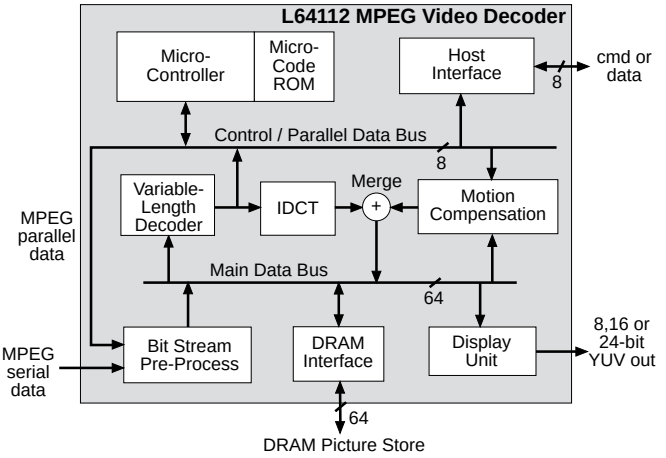

Figure 2. The 64112's microcode engine drives the special function units to perform the MPEG decoding algorithm.

