Literature Watch

Buses

RACE architecture brings flexibility to multiprocessing. Warren Andrews, Computer Design, May 1993, pg 44, 4 pgs.

Performance drives high-end bus standards. *VME is showing its age, but an infusion of new technology is expected to extend its life to the end of the decade. And while Futurebus+ and SCI are just emerging, designers are already looking to extensions.* Warren Andrews, Computer Design, May 1993, pg 59, 7 pgs.

Multiprocessor bus links µPs with 160-Mbyte/sec crossbars. Steven H. Leibson, Mercury Computer Systems; EDN, 5/13/93, pg 73, 2 pgs.

Development Tools

Design tools speed presynthesis system design. Doug Conner, EDN, 5/27/93, pg 85, 2 pgs.

VHDL—panacea or hype? *IEEE 1076—the hardware description language standard—is beginning to solve many long-standing IC design problems.* Michael Carroll, VHDL International; IEEE Spectrum, June 1993, pg 34, 4 pgs.

VHDL simulation takes leap forward. *Next generation of simulator technology improves speed from two to ten times.* Richard Pell Jr., Electronic Products, May 1993, pg 17, 2 pgs.

PLD programming modules manage adverse effects. *The fast edges and transmission line effects common with high-speed devices can create programming and test problems, but they can be tamed in the right environment.* Colin McCracken, Data I/O Corp.; Electronic Products, May 1993, pg 57, 4 pgs.

Signal integrity tools balance accuracy and ease of use. Mike Donlin, Computer Design, May 1993, pg 49, 3 pgs.

ROM emulators blaze path to low-cost debugging in the '90s. *You might call ROM emulators the poor relations of embedded-systems debugging. Nevertheless, these simple, useful, low-cost devices may offer a glimpse of things to come.* Dan Strassberg, EDN, 5/13/93, pg 53, 7 pgs.

Create optimal simulation libraries using VHDL. *One of VHDL's (VHSIC Hardware Description Language's) biggest drawbacks is that its power and flexibility allow too many solutions to any given modeling problem. However, by incorporating the following guidelines, you can create simulation models that are optimal and efficient.* Tonny Yu, Synopsys; EDN, 5/13/93, pg 133, 7 pgs.

DSPs

New applications driving dedicated DSP processors. *All-digital speaker systems, teleconferencing, medical imaging, and mechanical servos that position disk-drive read heads or levitate trains are the results of dedicated DSP chips and development tools.* Stephan Ohr, Computer Design, May 1993, pg 83, 10 pgs.

Graphics

Video DACs keep pace with GUIs and hi-resolution monitors. Jeffrey Child, Computer Design, May 1993, pg 101, 6 pgs.

Miscellaneous

Survey of commercial parallel machines. Gowri Ramanathan and Joel Oren, Oregon State University; Computer Architecture News, June 1993, pg 13, 21 pgs.

Physical limitations of a computer. Iraj Danesh, Computer Architecture News, June 1993, pg 40, 6 pgs.

Neural, fuzzy methods combine for embedded code generation. Tom Williams, Computer Design, May 1993, pg 36, 2 pgs.

Neural networks at work. *With specialized hardware available, neural networks frequently handle pattern recognition more effectively than traditional methods.* Dan Hammerstrom, Adaptive Solutions, Inc.; IEEE Spectrum, June 1993, pg 26, 7 pgs.

The picnic is over. *Slow growth, lower prices, and competition from more powerful PCs are putting pressure on workstation vendors. Sun Microsystems appears most vulnerable.* Bill Sharp, Electronic Business, June 1993, pg 101, 3 pgs.

Image compression. *Third in a 3-part series on image compression, this article looks at the proprietary algorithms that are available to licensing. Parts 1 (January 21) and 2 (March 4) discussed image-compression basics and the internationally standardized algorithms.* Richard A. Quinnell, EDN, 5/13/93, pg 114, 6 pgs.

Peripheral Chips

Battery-management ICs. *ICs that manage fast charging NiCd or NiMH batteries in 15 minutes also optimize service life and indicate charge status. In fact, these ICs may soon become an integral part of battery packs.* Brian Kerridge, EDN, 5/13/93, pg 100, 8 pgs.

Processors

80C51 microcontroller incorporates 4 Kbytes on-chip flash memory. Ray Weiss, EDN, 5/27/93, pg 98, 1 pg.

Motorola 68HC08 boosts 68HC05 speed, performance. Ray Weiss, EDN, 5/13/93, pg 88, 2 pgs.

System Design

Secondary cache performance in RISC architectures. Benjamin J. Ewy, Joseph B. Evans, Computer Architecture News, June 1993, pg 34, 6 pgs.

