Polar Sets New Direction for PDA Market

VLSI/Intel Collaboration Produces 386 Chip for Handheld Devices

by Linley Gwennap

VLSI Technology and Intel have announced the first fruit of their joint efforts in the PDA market. The Polar chip set combines a static 386 core with 2K of on-chip cache, memory control, and peripherals commonly used in handheld systems. It is not compatible with standard DOS or Windows but will support pen-based operating systems from Microsoft and Go. Polar is slated to begin shipments in 1Q94 and will eventually appear in a PDA from Compaq using the Microsoft At Work operating system (see "Mobile Companions" sidebar) as well as other portable devices.

Until now, upstart CPU vendors such as AT&T (with its Hobbit processor) and ARM have gained major PDA design wins. These initial signs indicate that PDAs might support a wider set of processors than the x86-dominated PC world.

Intel and Microsoft hope to change that impression and to dominate the PDA market as well. At Work is designed to allow software vendors to easily move their Microsoft Windows applications to a handheld platform. System designers that use an x86 CPU can take advantage of the wide range of compilers and other tools for that processor as well as the x86 design experience that many vendors have developed.

It is less clear what value an x86/At Work PDA offers to its users. Users may not appreciate having the "look and feel" of Windows applications on their PDAs; in fact, one of the fundamental purposes of a PDA is to attract users who are uncomfortable with traditional PCs. Even if Microsoft succeeds in creating a suitable interface, PDA buyers need good performance at a low price and with low power consumption, regardless of whose name is on the chip.

Intel believes that Polar will achieve about 6 Dhrystone MIPS at its top speed of 33 MHz. This is less than half the performance of Hobbit and ARM, although Polar has similar power requirements to its RISC-like competitors. One advantage that VLSI has is its price; at $50, a minimum Polar system is half the price of the Hobbit chip set. The ARM610 is much less expensive than Polar but the only system-logic chip for ARM is not openly available *(see **071303.PDF**)*.

The recent announcement provides the first detailed look at the VLSI/Intel chip set. It is difficult to evaluate, however, because VLSI has only recently received first silicon of the two parts; thus, power and performance numbers, key figures for the PDA market, are only estimates. In addition, several new PDA processors will be announced in the next month that may alter the competitive balance.

Complete PDA on Two Chips

Polar consists of two chips, the integrated processor controller (IPC) and the multiple peripheral controller (MPC), as shown in Figure 1. The two chips together provide nearly all the interfaces needed by a typical

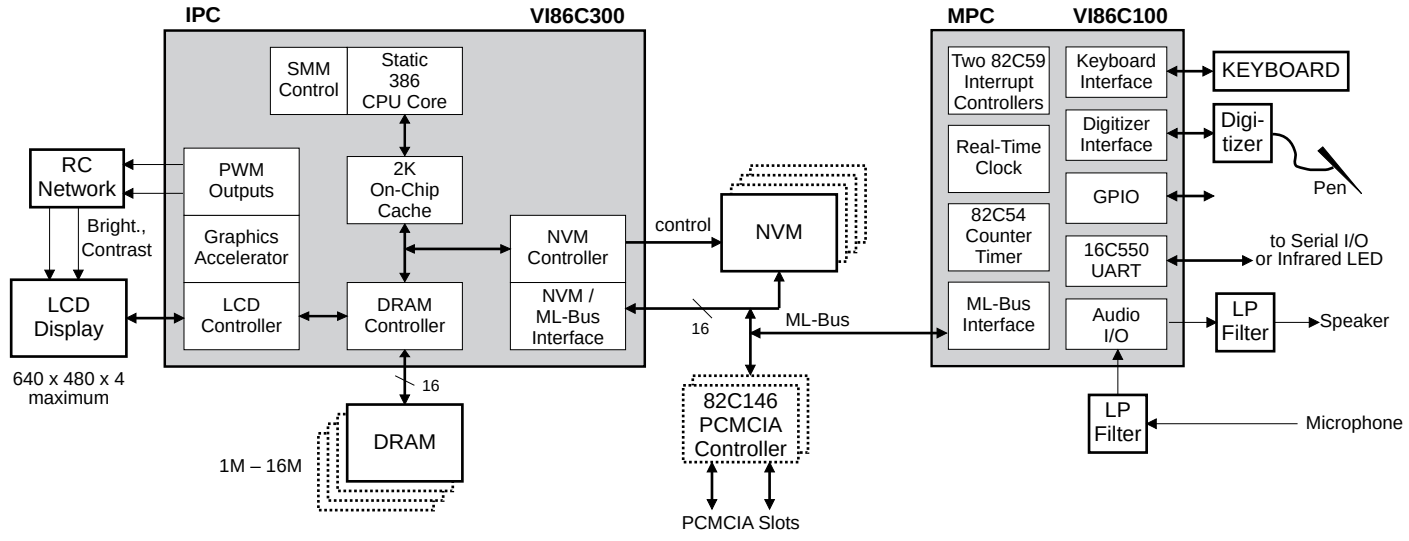

Figure 1. An entire handheld system can be built around the Polar chip set with a minimum of added components. The chip set supports various types of memory and peripherals directly; up to four PCMCIA slots can be added using VLSI's VL82C146.

Mobile Companions

Compaq announced plans to build a "mobile companion" based on the Polar chip set and a version of Microsoft's At Work operating system. The company released few details about the device, which is planned to begin shipping around the middle of next year. The name is meant to emphasize the system's role as a companion to the desktop PC, but the feature set is quite similar to current PDAs.

While the Compaq product will be the first to use Polar and At Work, Microsoft and Intel expect other companies to adopt their technologies and build devices compatible with Compaq's design. With Apple expanding its Newton licensing program *(see **071303.PDF**)* and AT&T working to establish the PenPoint/Hobbit platform, the At Work/x86 combination sets up a battle royale for the few current PDA suppliers.

handheld device. PCMCIA slots can be supported by adding VLSI's 82C146 controller chip *(see **070903.PDF**)*. There are no provisions for adding ISA-based peripheral chips, although the GPIO signals can be configured to emulate an 8-bit X-bus.

The chip set includes a wealth of features, making it likely that few, if any, peripherals would need to be added. The IPC contains an LCD display controller along with the CPU, cache, and memory control. The MPC includes counters, interrupts, and a real-time clock, along with connections for pen and keyboard input, serial devices, infrared output, a microphone, and a speaker.

Polar can operate at either 3.3 V or 5 V, but it gains no clock frequency advantage from operating at the higher voltage. Even with the CPU core running at 3.3 V, many of the interfaces have separate power inputs and can be operated at 5 V for compatibility with standard peripherals.

The IPC uses a 176-pin package and the MPC needs just 100 pins. Several techniques help keep the pin count low. There is no support for an off-chip cache, eliminating the need for a separate SRAM bus. Similarly, a separate bus for the frame buffer is not implemented; instead, graphics data is stored in DRAM alongside program data. A single bus allows the two Polar chips to communicate with each other as well as with nonvolatile memory and the optional PCMCIA chips. This 16-bit ML-Bus *(see **070903.PDF**)* multiplexes address and data signals to further reduce pin count.

Intel builds the IPC using a 0.8-micron, three-layer-metal CMOS process. This fairly mature process keeps manufacturing costs low and reduces power from Intel's 1.0-micron 386 chips. VLSI builds the MPC in 0.8-micron, two-layer-metal CMOS. Both Polar chips use thin quad flat packages (TQFPs), with a 0.5-mm pin pitch, to reduce the size of the devices. The IPC package measures 24 × 24 mm, while the MPC is even smaller at 14 × 14 mm. These small packages are well-suited for the handheld form factor.

The 0.8-micron process also reduces the die size. Since the Polar design is not final, VLSI would quote only the target die sizes; the company believes that the IPC will measure 84 mm^2 and the MPC will be 54 mm^2. By comparison, Intel's 386SL, which integrates fewer peripherals than Polar, measures 170 mm^2 using a 1.0-micron process. The MPR Cost Model *(see **071004.PDF**)* estimates that Polar chip set costs about $35 to build, about three times as much as a 386DX.

Modified 386 Core

Intel designed the CPU core for Polar starting with a 386SL core that already included static operation and system-management mode (SMM). The Polar CPU is said to be state-for-state compatible with a standard 386SX CPU, but power dissipation is greatly reduced due to the 3.3-V supply and smaller transistors. A few unneeded features, such as built-in self-test, were removed to further reduce power consumption.

Polar includes a 2K on-chip cache that holds both instructions and data. The primary function of this cache is not to increase performance, as in most other processors, but simply to reduce the number of accesses to main memory. Since graphics and program data are combined in DRAM, the single memory bus must handle traffic for both the CPU and the graphics subsystem. The on-chip cache frees enough bandwidth to provide adequate graphics performance. By reducing the number of DRAM accesses, it also saves power.

Polar uses a simple direct-mapped, write-through cache design to minimize gate count. The line size is eight bytes, but each 16-bit value has its own valid bit so the entire line does not have to be written each time a single word is updated. A four-word write buffer helps mask the DRAM latency and prevent the CPU from stalling on writes.

Memory and Graphics Combined

The DRAM bus is only 16 bits wide but can operate at up to twice the speed of the CPU to increase the bandwidth. With 80-ns DRAMs, a 25-MHz CPU has zero wait states on page hits. At 33 MHz, the system must use 60-ns DRAMs or accept one wait state. Up to 16M of DRAM can be installed using a variety of device types.

The DRAM memory is shared between the CPU and the graphics subsystem. The IPC contains a graphics accelerator and connects directly to a variety of gray-scale LCD displays with a maximum resolution of 640 × 480 × 4 bits per pixel. Future versions will support color LCDs as well. Two pulse-width modulation (PWM) outputs can be used to control the brightness and contrast of

the LCD display, as shown in Figure 1.

The graphics system uses a variable-size portion of the DRAM, depending on the display size and pixel depth. VGA emulation is not available, preventing Polar from running DOS. Due to the tight coupling of the graphics and memory subsystems, graphics performance is roughly equivalent to a local-bus frame buffer.

The IPC also contains an interface to non-volatile memory (NVM), which can be implemented using ROM, flash memory, battery-backed SRAM, or a combination of these devices. NVM data is transferred across a 16-bit multiplexed address/data bus, as shown in Figure 1, and can be cached. The separate buses for NVM and DRAM improve the performance of ROM-based software.

Integrated PDA Peripherals

While the IPC contains interfaces to high-speed devices such as memory and graphics, the MPC chip contains all of the lower-speed peripherals and system logic. It has the equivalent of dual 8259 interrupt controllers, an 8254 counter/timer, a real-time clock, and a 16C550 UART. In addition to standard serial protocols, the UART supports Hewlett-Packard's 95LX infrared protocol. The MPC also includes seven general-purpose I/O pins. Many of these features are similar to those in the Scamp IV notebook chip set *(see **070903.PDF**)*.

A few new functions have been added specifically for handheld devices. The MPC has a serial digitizer interface that is compatible with most digitizer chips, which detect the location of the pen when writing on the screen. The MPC also includes a 10-bit ADC and 10-bit DAC for audio I/O. When connected to a microphone and speaker through low-pass filters, these can provide voice-messaging functions.

Power Management Built In

Like most chips designed for portable applications (and like VLSI's own Scamp chip sets), Polar implements a variety of features that can be used for power management. System designers can choose to use some or all of them to minimize power consumption of the system.

Since Polar is fully static, it can retain its state even when the input clock is completely stopped. While the chip set is estimated to use about 600 mW at 33 MHz and 3.3 V, power will drop to under 100 mW in Doze mode (clocks stopped, peripherals powered). With the peripherals off, power usage will be a negligible 1 mW.

Peripherals and subsystems can be powered down individually when not in use. The chip set includes dedicated timers and activity monitors that help software determine when to turn off power to a unit. Power-management software can execute in SMM. The chip set also includes three analog inputs that can be used for voltage monitoring. The general-purpose outputs can be used to control off-chip peripherals.

Price and Availability

The Polar chip set consists of the VI86C300 (IPC) and VI86C100 (MPC). The IPC uses a 176-pin TQFP while the MPC uses a 100-pin TQFP. The price of the two-chip set is $50 in quantities of 10,000. VLSI expects to sample the chip set in 4Q93 with production in 1Q94. The VL82C146 PCMCIA controller, in a 100-pin TQFP, is currently available for $8.50 in quantities of 1,000.

Contact VLSI Technology at 8375 South River Parkway, Tempe, AZ 85284; 602.752.6226, fax 602.752.6008.

Attack of the Giants

PDA technology was pioneered by small, innovative companies such as Go, Eo, and ARM. As market fervor has grown and a few companies actually started shipping products, PDAs have attracted the attention of some very big companies. Go and Eo are now tucked under AT&T's corporate wing *(see **0712MSB.PDF**)* and ARM is closely tied to Apple. With Intel, Microsoft, and Compaq deploying PDA technology, the emerging market is clearly legitimized.

These PC giants may find it more difficult to dominate the PDA market, however. Polar lags existing PDA chips in pure performance and in performance per watt, an important metric in the handheld market. Although VLSI has opened a pricing gap against Hobbit, AT&T is planning to introduce next-generation chips that could close that gap before Polar begins shipping. The Hobbit chip set also supports four PCMCIA slots, while Polar requires additional parts for these slots.

Early next year, Intel and VLSI plan to introduce the Draco chip set, which provides the PDA functions of Polar for a standard 486 CPU. This should solve any performance problems but may not improve the MIPS-per-watt or MIPS-per-dollar rating of x86-based PDAs.

The PDA's user interface is an important factor in attracting a large customer base. Most people are not interested in running Excel spreadsheets on a four-inch LCD display. PDA applications will require new paradigms such as pen and voice entry, with objects that are intuitive and easy to manipulate. Both Newton and Go's Penpoint are built from scratch to deal with these issues. Microsoft will have to develop something new to be successful in PDA software.

VLSI itself is well positioned in the PDA market, as it also supplies ARM processors to Apple for its Newton PDA. By developing chips for x86-based PDAs, the company can ride two horses in the same race and hope that one of them comes home victorious. ♦

Our inaugural (10/18/93) issue of MicroSystems Insider *will feature an article on system design using the Polar chip set.*

