Most Significant Bits

IBM Announces First PowerPC Systems

IBM has raised the veil on the first system using the PowerPC 601 processor. The RS/6000 Model 250 delivers 62 SPECint92 and 72 SPECfp92 using a 67-MHz CPU *(see **071301.PDF**)*. The base price of the system is $4,795, but this does not include a disk or monitor. A more useful configuration—32M of memory, 540M disk, and a 17" color monitor—is priced at $15,400. The Model 250 will begin shipping in October.

The PowerPC system delivers higher integer and floating-point performance than similarly priced entry-level systems from HP, Sun, and Digital. For example, the Digital Model 300L is rated at 46 SPECint92 and 64 SPECfp92, with a configured cost of about $15,000. While the 601 does not match the performance of competitors' higher-cost systems, IBM also announced new systems based on its Power2 processor that take a performance lead at the high end *(see **071301.PDF**)*.

Even the older, Power1-based systems have been improved. New compilers boost the SPECint92 performance of these systems by up to 18%. For example, the highest-speed Power1 system—the 62.5-MHz Model 580—is now rated at 73 SPECint92, up from 62. While this still leaves Power1 lagging the Alpha 21064, R4400, and PA7100 in integer performance, IBM plans to move the more powerful Power2 into its desktop products in 1H94 to close this gap.

Also scheduled for release next year are 601-based PCs from IBM's new Power Personal Systems group. The company demonstrated WABI (Windows ABI) software that it has licensed from Sun. IBM claims WABI will allow a 601 PC to run off-the-shelf Windows applications at the speed of a 486DX2-66. Combined with Apple's Macintosh emulation software and a unified UNIX API (see below), these PowerPC systems could run nearly any application. There is still no official word about NT-on-PowerPC, but IBM says it will support any industry standards to meet customer demand.

AMD Used Dirty "Clean Room"

In a surprise announcement, AMD has revealed that its "clean room" 486 microcode *(see **0709MSB.PDF**)* isn't quite clean: the design team had access to Intel's 386 microcode during the development process. At the time, the company believed it had rights to that Intel code, and AMD chose to use it in the 486 microcode development process to get to market more quickly. After the Court of Appeals overturned the arbitration award in June, however, AMD was forced to begin a second clean-room effort to rewrite the microcode without any Intel influence.

The microcode incident once again demonstrates AMD's lack of contingency planning for adverse court rulings. AMD VP Robert McConnell conceded that AMD's thinking had been "too colored by being sure that we were right," and he said that the company would not again make the mistake of assuming that legal decisions would reflect this belief.

The original 486 clean-room microcode got a late start because AMD did not believe it would lose the original 287 microcode case, but it did *(see **060901.PDF**)*. Now, AMD will have to rewrite its microcode again as insurance against possible future negative legal opinions. As CEO Jerry Sanders said repeatedly at a press conference, "At AMD, we know how to write microcode." They should, having done it far too many times.

The revelation hurts AMD's credibility; it apparently knew that its microcode was tainted but did not disclose this fact at its July announcement. This has already prompted a shareholder lawsuit. Company officials said that their legal department would not allow them to explain further, but that they believed their July clean-room announcement to be accurate when they made it. From the available information, it is not clear how this could be the case.

AMD said that 486 sales remain strong, with well over 150,000 chips to be shipped this quarter and over 400,000 projected for the fourth quarter. Although no foundry announcements have been made, AMD says that it can ship at least 4 million units next year from its Submicron Development Center in Sunnyvale.

Court Overturns Reversal of AMD Ruling

Further complicating the Intel/AMD situation, the California Supreme Court has agreed to hear arguments in the ongoing legal battle over the arbitration ruling regarding the 386. Previously, the California Court of Appeals had overturned the arbitrator's ruling that granted AMD the right to sell 386 chips based on Intel's designs *(see **0708MSB.PDF**)*. The Supreme Court's acceptance of AMD's appeal legally negates the appellate decision. The Supreme Court accepts relatively few cases, so its action in this instance is a positive sign for AMD.

The decision gives AMD breathing room to develop its new, squeaky clean microcode (see previous item). By overturning Intel's earlier victory, the Supreme Court ensures that AMD's 386 sales cannot be challenged until the court makes a final ruling on the case, which is not expected until next fall.

For AMD's shareholders, however, the worst-case outcome is more serious: if AMD loses both the Supreme Court appeal and the pending 287 microcode case *(see **070601.PDF**)*, then it could be liable to Intel for all the profits it has earned on its 386 and 486 chips. If the Supreme Court rules in AMD's favor but the 287 case

goes against AMD, AMD could be liable to Intel for all profits on its 486 chips using Intel microcode.

NEC Announces 0.5-Micron 8086 Core

NEC has expanded its line of 8086-compatible processor cores with the V30MX, which operates at up to 33 MHz with a 3-V supply. The new core is upward-compatible with NEC's V20HL and V30HL. It supports up to 16M of memory space using a 24-bit address bus. The V30MX offers a significant performance upgrade from its predecessor; at 33 MHz, the new core delivers 2.8 times the performance of a 20-MHz V30HL. Power consumption is quite low: 27 mA at 33 MHz.

The new core will be available as part of a 3-V, 0.5-micron family of ASICs called CB-C8. Customers can combine the V30MX CPU with as many as 600,000 user-defined gates using three metal layers for interconnect. Alternatively, some of the die area can be used for standard cells such as RAM, ROM, or PLLs. NEC's library also includes megacells for DMA and interrupt controllers, as well as floppy-disk and other peripheral interfaces. CB-C8 can support 3-V, 5-V, or LVTTL I/O signals. The small transistors and low voltage reduce the power dissipation of each gate to 0.8 µW/MHz.

NEC is aiming its new technology at customer-specific applications in portable communications and other consumer devices. These areas can take advantage of CB-C8's increased integration and low power consumption. It could even be used for PDAs or pocket PCs, although it may be underpowered for these types of products. Design fees and unit prices for CB-C8 vary depending on the complexity of the device; NEC is currently accepting designs for this new technology.

VLSI Offers Integrated ARM Processor

To expand its ARM ASIC business, VLSI has put together a "customizable microcontroller" based on the ARM6 core (see MPR 12/18/91, p. 8). The VY86C650 includes a 4K cache, memory controller, DMA controller, interrupt controller, timers, parallel port, serial port, and laser-printer video interface. All of these functions are implemented as ASIC library elements in Verilog HDL, allowing customers to easily produce their own configurations as needed.

ARM has well-publicized design wins at 3DO and in the Newton *(see **071303.PDF**)*, but the ARM core has been finding its way into other embedded applications as well, including some audio/video processors and peripheral controllers. VLSI hopes the new part will help penetrate new markets; in particular, the video interface should allow the 86C650 to compete in the laser-printer market. The basic version of the chip is priced at $60 in quantities of 100; customized versions require a variable up-front design fee.

Interleaving Boosts Performance of S3 805i

S3 has upgraded its 805 graphics accelerator with the 805i. The new chip uses an interleaved frame buffer, much like Tseng's W32i *(see **070901.PDF**)*. The 805i supports up to 2M of DRAM—twice that of the 805—allowing resolutions up to 1280 × 1024 × 8. The interleaved memory also increases performance. The 805i supports the power-saving DPMS protocol for "green PCs." Like the 805, the new chip connects directly to the ISA, EISA, or VL-Bus.

The 805i is priced at $28 in quantities of 10,000 per quarter, only a $3 premium over the original 805. It is pin-compatible with its predecessor, offering an attractive upgrade to the popular graphics accelerator. S3 continues to offer the more costly 928 *(see **061202.PDF**)* as its high-end solution.

Another UNIX Unification Announced

This time, they've finally agreed on a standard API. The companies behind the COSE standardization efforts, and a few of their friends, announced a common programming interface that they all agreed to support. Backers include Sun, IBM, HP, Digital, Novell, and the Santa Cruz Operation—over 75 vendors in all. The common API (CAPI), based on System V Release 4 (SVR4), will be administered as part of the X/Open Portability Guide 4 (XPG4).

A single API will allow application vendors to easily port their software from one UNIX platform to another without the complex and often buggy set of "if-defs" needed to handle the peculiarities of each system. UNIX utilities will also be ported more easily from kernel to kernel. No time for hallelujahs yet; vendors' plans to add CAPI support to their operating systems range from 1H94 to "no schedule yet."

National Unveils First QuickRing Chips

National Semiconductor has unveiled its QR0001 QuickRing interface chip, marking the formal debut of this new interface technology. QuickRing originated at Apple, but Apple's interest has waned and National is now carrying the ball. While the design has its basis in the Scalable Coherent Interface (SCI), it is not part of any IEEE standards effort.

QuickRing, which achieves a sustained bandwidth of 200 Mbytes/s, is intended to serve as a high-speed interconnect for digital video systems and other computer peripherals whose bandwidth requirements outstrip existing standards. It can be used as an "airplane" bus, connecting to the top edge of add-in cards whose bottom edge plugs into a lower-speed standard bus, or it can be used as an inter-box connection with a maximum length of about three meters.

One of the QuickRing precepts is that buses won't be able to keep up as speeds increase. The electrical

stubs inherent in a multi-drop bus are a nightmare for high-frequency signal quality, limiting their usefulness above 80 MHz or so. QuickRing is a point-to-point interconnect, allowing up to 16 devices to be connected in a ring. Each signal is carried on a differential pair, using ±150 mV thresholds (conforming to IEEE P1596.3).

A QuickRing data path consists of six data signals and a 50-MHz clock signal. Using an unusual clocking scheme, the data rate is seven times faster than the clock rate. Each receiver uses a phase-locked loop and delay line to generate seven sampling times for each clock cycle, resulting in a data rate on each line of 350 Mbits/s, or a peak rate of 263 Mbytes/s for the six data signals. After protocol overhead, the deliverable bandwidth is 200 Mbytes/s. Because the point-to-point design allows multiple concurrent transmissions, a 16-node ring can sustain data rates of up to 1700 Mbytes/s.

National's QR0001 data stream controller provides one QuickRing receive port and one QuickRing transmit port, providing a complete interface for one node. Deep FIFOs buffer the host port from the high data rate. The 160-pin chip has a complexity of about 35K gates and dissipates 2.2 W maximum. Samples will be available in October, with production promised by December. In 1000-piece quantities, the QR0001 is priced at $45.

National's vision is for QuickRing to take a major role in future PC architectures, eventually replacing CPU local buses for high-end graphics and other high-speed peripherals. National also hopes that it will perform the same role as SCSI for high-performance devices. It may be many years before mainstream applications outstrip the capabilities of cheaper buses such as SCSI and PCI, but for applications that need higher bandwidth, QuickRing is one of the few off-the-shelf solutions and could become popular.

C-Cube Has Real-Time MPEG-2 Encoder

Already the video compression leader, C-Cube affirmed its position by announcing the first chip set to perform MPEG-2 encoding in real time. The CLM4600 can encode video signals at resolutions up to 704 × 576, more than four times the pixel count of MPEG-1 and suitable for television broadcast standards. The new system can be used for MPEG authoring, satellite uplinks, and local cable head-ends to provide advanced video services.

The chip set uses 8–10 CL4000 video processor chips. Each chip includes a 60-MHz RISC processor that can perform signal-processing operations on four words in parallel, or 240 million operations per second. Two coprocessors handle the motion estimation and Huffman encoding operations required by the MPEG algorithm. Separate instruction and data caches of 4K each keep memory bandwidth high.

The CL4000 chips can be connected in parallel, dividing the video image into slightly overlapping strips, to provide the desired level of performance. A low-end system with just two chips, for example, could perform real-time MPEG-1 encoding or MPEG-2 encoding at less than real-time speed. The chips are also programmable to handle other algorithms such as JPEG and H.261.

C-Cube is currently sampling the CL4000 for NTSC applications and will be able to handle PAL systems by the end of the year. Since the total market size for this product is measured in thousands of units per year, C-Cube is charging a steep price: $10,000 for samples of the ten-chip set. Systems using the new chips replace encoding devices that cost as much as a million dollars, so the new solution is cheap even at that price. ♦

