Literature Watch

Buses

High-speed bus interfaces. *As system speeds begin to exceed 50 MHz, the faithful old TTL interface starts running out of steam. A variety of alternative interfaces can take on high-speed-system needs. No single option, however, will dominate the industry as TTL did.* Richard A. Quinnell, EDN, 9/30/93, p. 43, 7 pp.

New bus wars starting to flicker. *What will succeed VME?* Warren Andrews, Computer Design, 9/93, p. 22, 3 pp.

VME P2 target of heated ANSI standards activity. Warren Andrews, Computer Design, 9/93, p. 40, 2 pp.

Will 1994 be the year of Futurebus+? *Futurebus+, like the bear climbing the mountain in the children's song, continues to cover ground only to see another mountain. Cache coherency, the telecom profile, and military COTS form factor loom ahead.* Warren Andrews, Computer Design, 9/93, p. 49, 8 pp.

Development Tools

Debugging in the 8-bit world. *You now have many tools to choose from to debug your 8-bit µP-based project, but each one has its strengths and weaknesses. Avoid major headaches by taking time to learn the differences before you begin a project.* David Shear, EDN, 9/16/93, p. 69, 4 pp.

Accurate timing analysis holds the key to performance in today's system designs. *Back when systems loafed along at 10-MHz clock speeds, designers could cure timing problems by using faster chips in trouble spots. They no longer have this easy way out—in today's designs, fast clock rates make highly accurate system timing a crucial design parameter.* Bruce Gladstone, Chronology Corp.; EDN, 9/16/93, p. 137, 9 pp.

68360 QICC gets emulator support. Jeffrey Child, Computer Design, 9/93, p. 118, 1 p.

ICE for Pentium runs at full 66-MHz. *Microtek's new emulator for the Intel Pentium processor runs at the full 66-MHz clock speed of the chip, gives access to all internal registers as well as instruction trace in the cache, and provides a Windows-based user interface.* Tom Williams, Computer Design, 9/93, p. 116, 1 p.

DSPs

Multiprocessor DSP system presents rigorous computational-latency demands. Winthrop W. Smith, E-Systems; Personal Engineering & Instrumentation News, 9/93, p. 63, 3 pp.

EDN's DSP-chip directory. *EDN's revamped DSP-chip directory takes a page from our Microprocessor Directory by providing at-a-glance performance, architectural, and pricing data for 19 chips.* Ray Weiss, Technical Editor, Julie Anne Schofield, Senior Associate Editor, EDN, 9/30/93, p. 57, 21 pp.

DSP^x showcases digital-signal-processing products. Susan Rose, EDN, 9/16/93, p. 15, 2 pp.

Memory

Low-power DRAMs head for mainstream. *Because most DRAM makers need to use the 16-Mbit process technology to achieve 3.3-V, the transition from 5 V to 3.3 V will speed up DRAM vendors' efforts to bring their 16-Mbit process technology up to full volume. By 1996 the DRAM market will be dominated by 3.3-V parts.* Jeffrey Child, Computer Design, 9/93, p. 105, 5 pp.

Miscellaneous

Sun takes on the world. *The workstation market leader wants to be seen as a general-purpose network-computing supplier. Does Sun have what it takes?* Natalie Engler, UnixWorld, 10/93, p. 51, 3 pp.

After Windows NT, engineering will never be the same. *If Microsoft's Windows NT performs as advertised, computer-aided engineering will never be the same.* Charles H. Small, EDN, 9/30/93, p. 35, 4 pp.

Microcontrollers embrace fuzzy logic. *Most current fuzzy-logic applications run very nicely on general-purpose microcontrollers. For very demanding applications, you can turn to special-purpose fuzzy chips.* Gary Legg, EDN, 9/16/93, p. 100, 7 pp.

Peripheral Chips

Chip set marks turning point for twisted-pair FDDI. Jeffrey Child, Computer Design, 9/30, p. 30, 3 pp.

Processors

8-bit PIC µC moves to the midrange with timers, 33 I/O pins. *The PIC16C64 delivers 200-nsec pipelined instruction execution combined with two timers, 2K-word instruction EPROM, 128 bytes of register RAM, and up to 33 I/Os.* Ray Weiss, EDN, 9/30/93, p. 142, 2 pp.

Mitsubishi 16-bit µC reduces power consumption. *Mitsubishi's M7702L6 16-bit µC can run at 25 MHz and keep typical power below 100 mA. The µC has 48 Kbytes of ROM, 2 Kbytes of ROM, 2 Kbytes of RAM, an ADC, and eight 16-bit timers.* Ray Weiss, EDN, 9/30/93, p. 143, 1 p.

IBM sheds light on embedded PowerPC 400 series. Jeff Child, Computer Design, 9/93, p. 28, 1 p.

Programmable Logic

10-nsec complex PLD blends four 24V10 PALs on chip. Ray Weiss, EDN, 9/30/93, p. 135, 1 p.

System Design

SPARC offerings multiply. Warren Andrews, Computer Design, 9/93, p. 36, 3 pp.

Designing non-volatile memory systems. Sandy Scherpenberg, Dallas Semiconductor; Computer Design, 9/93, p. 127, 2 pp.

