ARM7 Cuts Power, Increases Performance

New ARM700 Challenges Hobbit for PDA Performance Lead

by Linley Gwennap

With many initial Newton customers wishing for better performance and longer battery life, Advanced RISC Machines (ARM) is already solving these problems. At last month's Microprocessor Forum, ARM's Mike Muller unveiled the ARM7 family, offering both performance improvements and lower power compared with the ARM610, which is used in the current Newton. The new chips could appear in Apple PDAs as early as the middle of next year.

ARM7 processors are based on a redesign of the ARM6 core that takes advantage of 0.8-micron technology (the ARM6 uses a 1.0-micron process). This IC process is now mature enough to offer the low cost demanded by ARM. Few changes were made to the logical design; the new process, however, is enough to deliver a 33% increase in clock speed and a comparable decrease in power. Unlike the ARM610, the new parts will run at 3 V, further reducing power.

MICHAEL MUSTACCHI

"You can do wonderful things with a half-micron process, but you still have to pay for it."

Mike Muller, ARM

New Debug, Signal-Processing Features

Like previous generations, the ARM7 family starts with an ARM core. By redesigning the ARM6 core, the company was able to reduce the die area by nearly half, to less than 6 mm^2. Simply shrinking the core would have cut the area by about 30%; the redesign achieved better results by eliminating about 5% of the ARM6 transistors and compacting the rest.

The design team created two new functional blocks that are optional additions to the basic core. The first, called Icebreaker, allows an external debug monitor to directly access the ARM core, even if it is embedded within a complex ASIC. Unlike conventional debuggers, Icebreaker can be used before system I/O is available to access internal address and data buses and to breakpoint ROM-based code. It is accessed through the JTAG port, requires no additional pins, and adds only a few hundred transistors to the core.

Name	Description of Product
ARM7	ARM7 ASIC core
ARM7D	ARM7 core, Icebreaker-compatible
ARM7DM	ARM7 core with fast multiplier, Icebreaker-compatible
ARM70DM	ARM7DM core with Icebreaker in 128-pin MQFP
ARM700	ARM7 core with 8K cache, MMU, write buffer, and bus interface in 160-pin PQFP
ARM710	Same as ARM700 except in 144-pin TQFP

Table 1. ARM7 is available as an ASIC core, a simple CPU, or a complete processor with cache and MMU.

The second new block is a fast integer multiplier. It uses an early termination algorithm, and thus can complete an $8 \times 8 \rightarrow 8$-bit multiply in a single cycle. A $32 \times 8 \rightarrow 32$-bit multiply takes two cycles, while a full $32 \times 32 \rightarrow 32$-bit multiply completes in five cycles.

To take advantage of this multiplier, the ARM7 instruction sets adds new $32 \times 32 \rightarrow 64$-bit instructions; these can also perform multiply-accumulate using the form $R1 \times R2 + (R3,R4) \rightarrow (R3,R4)$, where R3 and R4 are a pair of registers that receive the 64-bit result. Unlike Icebreaker, the multiplier adds a significant number—about 10,000 or nearly 30%—of transistors to the core.

Muller believes that the new multiplier will be useful in medium-performance digital signal-processing applications. With the multiplier, he claims the ARM7 will be able to perform 140 1K FFTs per second; this is comparable to the speed of a TI 320C10 DSP, for example. For higher-end applications, the ARM processor can be coupled with a traditional DSP chip.

The ARM7 core is available as an ASIC macrocell or as part of the ARM7 processor chips. Table 1 shows the naming scheme for the various combinations of the basic core, Icebreaker, and fast multiplier.

ARM 700 to Succeed ARM610

The ARM610 was put together fairly quickly to meet Apple's needs. This haste created two problems with the chip. First, redesigning the MMU to meet Apple's specifications created a new critical path in the 610; although the ARM6 core operates at 25 MHz at 5 V, the 610 is limited to 20 MHz. Second, unlike most other processors designed for portable systems,the 610 was never qualified for operation at low voltages because its cache-sense amps do not operate below 5 V.

The new ARM700 processor fixes both of these problems. The 610 critical path occurs when the processor serially accesses the MMU and the on-board cache in a sin-

gle cycle. The new processor performs these two accesses in parallel, thus eliminating the delay. This allows the 700 to reach the same clock rates as the ARM7 core. The company has also redesigned the cache to operate at voltages down to 3 V.

To improve performance over the 610, the 700 includes other new features. The size of the on-chip cache is doubled to 8K. To keep pace with the larger cache, the number of entries in the TLB and write buffer are also doubled, to 64 and four respectively.

As shown in Table 2, the ARM7 processors are rated at 30 MIPS running at 5 V. Even at 3 V, performance is rated at 18 MIPS. Interestingly, the ARM7 delivers 65% better performance than the ARM6 at the same clock speed based solely on compiler improvements (since Dhrystone is not affected by the increase in cache and TLB sizes). It is not clear whether these compiler tweaks will deliver similar performance increases on real applications; the object-oriented Newton OS, for example, has much poorer cache locality than Dhrystone.

Without a doubt, the 700 will be significantly faster on applications than the 610, even if only the higher clock speed and larger on-chip memory are considered. The new chip will give Apple the option of building a Newton with much better performance than the current model while operating at 5 V, or of changing the CPU to run at 3 V while still improving performance over the current Newton. Although the latter move would reduce system power usage and extend battery life, the change may not be significant unless other system components are also configured to operate at low voltage.

GEC Plessey has announced sampling for the ARM700 with volume pricing set at $35 in 10K quantities. Since ARM only recently received first silicon of the ARM7, volume shipments are not expected until 2Q94. Plessey is currently supplying most of the ARM chips used in Newton systems. VLSI Technology and Sharp also plan to market the ARM700. TI recently licensed ARM technology but is mainly interested in the embedded market; it has rights to the ARM7 core but not the 700-family processors.

ARM Grabs Performance Lead

The ARM700 has a better Dhrystone MIPS rating than all other announced PDA processors. Its closest competitor is AT&T's 92020S Hobbit processor *(see **071403.PDF**)*, shown in Table 2. NEC's V810 and Hitachi's SH7000, other RISC-like processors, offer significantly lower performance than the ARM700. CISC-based PDA chips, such as Intel's Polar and Motorola's 68349, deliver about one-third of the performance of the ARM chip on Dhrystone.

Power is another important metric for these processors. With its new 3-V capability, the ARM processor is now among the leaders in this category as well, using just 120 mW. Without information on ARM support chips, however, it's impossible to compare power at the system level, which is more meaningful. At $35, the ARM700's list price is comparable to that of other PDA processors. It's difficult to compare the ARM CPU to the highly integrated Polar, which costs $50 but includes a complete set of PDA system logic and interfaces *(see **071302.PDF**)*.

Manufacturing cost ultimately determines the price given to large customers such as Apple. The tiny die size of the ARM700 gives it an estimated cost of about $14, according to the MPR Cost Model *(see **071004.PDF**)*. This is about the same as the ARM610; the smaller die compensates for the higher wafer cost of the 0.8-micron process. The table shows that the ARM chip holds a significant advantage over Hobbit in manufacturing cost, and thus should sell in volume for a much lower price.

One advantage for Hobbit and Polar is the open availability of complete PDA system-logic chip sets for these processors. Apple has said that it will make its Newton ASIC available only to its partners. Thus, at least for Apple and its friends, the ARM700 should be a competitive solution in the nascent PDA market. ♦

Price and Availability

GEC Plessey Semiconductors (GPS) is the first company to announce availability of the ARM700. The part is sampling now, with volume shipments expected in 2Q94. Pricing is $35 in quantities of 10,000. The other ARM semiconductor partners are expected to offer ARM7 products as well.

Contact Advanced RISC Machines at 44.0223.813.000, fax 44.0223.812.800 (UK).

Contact GEC Plessey Semiconductors at 44.0793.518.418, fax 44.0793.518.411 (UK).

Contact VLSI at 602.752.6373, fax 602.756.6001.

Contact Sharp at 206.834.8966, fax 206.834.8903.

Contact TI at 713.274.3368, fax 713.274.2573.

	ARM 610 (at 5 V)	ARM700 (at 5 V)	ARM700 (at 3 V)	92020S (at 3.3 V)
Frequency	20 MHz	33 MHz	20 MHz	20 MHz
Dhrystone 2.1	11 MIPS	30 MIPS	18 MIPS	16 MIPS
Power*	500 mW	550 mW	120 mW	210 mW
MIPS per Watt	22	55	150	76
Cache Size	4K	8K	8K	6K
TLB Entries	32	64	64	64
Die Area	71 mm^2	46 mm^2	46 mm^2	125 mm^2
Est. Mfg. Cost	$13	$14	$14	$24
List Price	$20	$35	$35	$37
(quantity)	(10K)	(10K)	(10K)	(10K)

Table 2. The ARM700 delivers higher performance at low voltage than AT&T's 92020S or any other announced PDA processor. *Power usage is with a 50-pf load under typical conditions.

