Texas Instruments Extends 486 Line

486SXL2, SXLC2 Add 8K Cache, Clock Doubler to 486SLC Core

by Michael Slater

TI, which has been an alternate source for Cyrix's 486SLC and 486DLC, has introduced its first internally designed derivatives of the Cyrix CPU core. The new TI chip adds an 8K, write-through cache to the Cyrix core and is offered in either a 486SLC (extended 386SX) or a 486SX pinout.

Both versions of TI's chip offer software-enabled clock doubling. The fastest parts (40 MHz at 3.3 V or 50 MHz at 5 V) aren't able to run the bus at the full CPU speed, so they must be operated in clock-doubled mode.

Intel has ignored the market for faster processors using the 386SX pinout, which is preferred by subnotebook designers because of its small size. The 486SLC has found a successful niche by giving makers of products such as HP's OmniBook a higher-performance alternative to the 386SX, combining a near-486-class CPU core and a small cache in a low-cost, 16-bit package. TI's 486SXLC2 takes this one step further by increasing the cache size to 8K and providing an optional clock doubler. It takes, at least for the moment, the performance lead among merchant-market processors in the 16-bit 386SX package, and this could make it a significant success. (IBM's 486SLC2 is faster, but can't be sold except as part of a system or subsystem.)

TI's 486SXL2 is the same die as the 486SXLC2, but in a 486SX-compatible pinout. Here, too, there is an opportunity to fill a gap left by Intel, which has offered clock doubling only in the 486DX version. Intel's strategy is designed to limit high-performance systems to its highest-profit chips. For many users, however, integer performance is far more important than floating-point, and a 486SX2-type product is appealing.

MICHAEL MUSTACCHI

"With modular core technology, TI is well-positioned to support superportable systems in the 1996 timeframe."

Ian Chen, TI

TI's 486SXL2, while meeting the basic description of Intel's missing 486SX2, falls short in two respects: the CPU core, which is unmodified from that in the 486SLC/DLC, is slightly slower than Intel's 486 core, and the bus interface does not support burst transfers. Essentially, this chip implements a 386DX-like bus interface in a 486DX pinout. Because of these weaknesses in TI's 486SXL2, AMD's 40-MHz 486SX and rumored 486SX2 are likely to be more successful. TI's chip must run at a higher clock rate than Intel's or AMD's 486 to deliver the same performance.

Table 1 compares the performance of the Intel and TI chips. While the SXLC-33 falls 4–19% short of Intel's 486SX at the same clock rate, the SXLC2-50 easily outperforms the SX-33, and the SXL2-50 widens the gap even further.

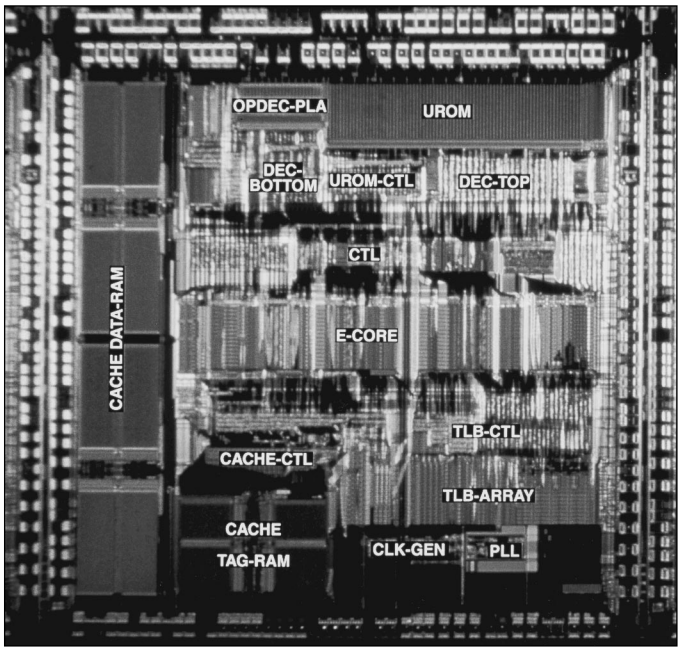
Both the SXL and SXLC will be available in 3.3-V and 5-V versions. At 3.3 V, clock rates supported are 33 MHz or 20/40 MHz (internal/external). At 5 V, the clock rates are 33 MHz or 25/50 MHz for the SXLC, and 40 MHz or 25/50 MHz for the SXL.

The chip incorporates about 900K transistors with a die size of approximately 130 mm^2 (200K $mils^2$) in a 0.8-micron, two-level-metal CMOS process. This is much larger than Intel's 486SX, which is only 72 mm^2 but uses a more expensive three-level-metal process. The MPR Cost Model *(see **071004.PDF**)* estimates the 486SXLC manufacturing cost to be $37, almost double the $19 estimated cost of Intel's 486SX.

Typical power consumption is less than 1 W at 3.3 V with a 33-MHz clock, or less than 2.5 W with a 40-MHz clock and a 5-V supply. With the clock stopped, typical current drain is below 20 µA. For comparison, Intel's 486SX-33 at 3.3 V has a typical power consumption of 990 mW; at 5 V and 33 MHz, it is just under 3 W. Thus, the TI and Intel chips use roughly the same power to deliver

	PowerMeter 1.7		LandMark 2.0		PC Mag 6.0 (486 Mix)	
	Rating	Relative to i486SX-33	Rating	Relative to i486SX-33	Rating	Relative to i486SX-33
i486SX-25	11.2	76%	84	75%	1040	75%
TI486SXLC-33	11.9	81%	103	92%	1337	96%
i486SX-33	14.7	100%	112	100%	1386	100%
TI486SXL-40	15.2	103%	130	116%	1698	123%
TI486SXLC2-50*	17.1	116%	156	139%	1830	132%
TI486SXL2-50	18.1	123%	162	145%	2035	147%

Table 1. Performance of TI's 486SXL2 and 486SXLC2, relative to Intel's 486SX. *Estimates. (Source: TI)



Die photo of TI's 486SXL/SXLC, which includes 900K transistors on a 130 mm² die.

Price & Availability

Samples of the 486SXLC2 and the 486SXL2 are available now, with production planned for 1Q94. Pricing in quantities of 1000 for the 486SXLC-33 is $79; the 486SXLC2-50 is $110. The 486SXL-33 is $89, while the 486SXL2-50 is $149. The above prices are for the 5-V versions; 3.3-V devices will be priced at about the level of the next-highest 5-V speed grade. Eventually, TI expects 3-V prices to approach 5-V prices.

Contact your local TI sales office or call 800.477.8924, ext. 3726.

equivalent performance.

The TI chips are fully static and include a system-management mode (SMI interrupt and address space) identical to that implemented in recent Cyrix devices.

Like all chips with phase-locked-loop clock doublers, the clock frequency cannot be changed rapidly. The TI chips allow the clock-doubling function to be software controlled, however, so software can switch the chip out of clock-doubled mode for power-management purposes, and then return it to that mode for maximum performance. The clock can also be stopped at the output of the PLL to put the chip into a low-power standby mode without incurring the start-up delay (which is less than 20 µs) that would be required if the PLL were stopped.

Cyrix, TI Paths Diverge

As Figure 1 illustrates, Cyrix and TI have pursued separate paths in producing derivatives of the 486SLC/DLC. The original 486SLC has a 1K, write-through cache and a 386SX-compatible pinout. The 486DLC, which uses the same silicon, provides a 32-bit bus in a 386DX-compatible pinout. Both Cyrix and TI sell these two devices, although Cyrix is focusing on the SLC version and TI has taken most DLC sales.

Cyrix has added a 2K write-back cache for its 486SX version, and an 8K cache for its 486DX equivalent. TI does not yet have a 486 with on-chip floating-point.

Cyrix is scheduled to announce today its clock-doubled version of the 486SLC, called the 486SLC2. (Note that the Cx486SLC2 is an entirely different chip from IBM's 486SLC2, although it is similar in concept.) Cyrix's SLC2 is very similar to TI's SXLC2, except that it has a smaller on-chip cache. Presumably, Cyrix will price it more aggressively than TI's chip, since TI will have a performance advantage.

Most of Cyrix's chips are fabricated by SGS-Thomson; while Cyrix also has a foundry agreement with TI, the relationship between the two companies has been contentious, and Cyrix says that its business plan is now based on getting no further silicon from TI.

One aspect of the Cyrix/TI dispute is over TI's rights to Cyrix designs beyond the original 486SLC/DLC, and this may be one reason why TI developed the 486SXL rather than simply making Cyrix's 486SLC2, 486S, and 486DX designs. Creating a derivative design gives TI a proprietary product, and it is also a first step toward

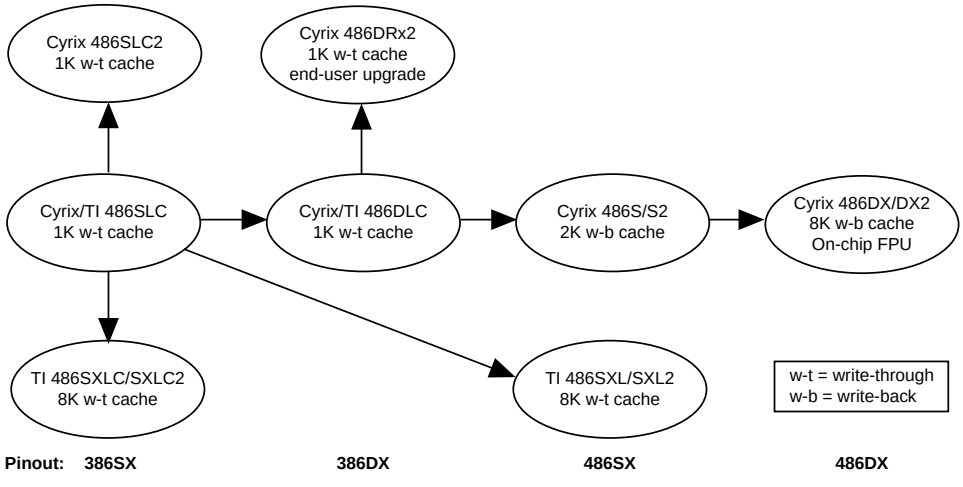


Figure 1. Texas Instruments and Cyrix have developed different derivatives from the 486SLC core.

VMT Offers Enhanced 386SX

V.M. Technology (VMT) founder Masatoshi Shima described at the Microprocessor Forum his company's enhanced 386SX-compatible microprocessor. VMT was founded by Shima, who was the chief designer of Intel's 8080 and Zilog's Z80 and Z8000. Financial backing has come from K. Nishi's ASCII Corp. and from the trading company Mitsui & Co.

The VM386SX+ is based on a VMT-designed CPU core that is instruction-set-compatible with the 386 but uses a more aggressive microarchitecture to increase performance. Performance on system-level, PC-oriented benchmarks is 5–15% better than a standard 386SX at the same clock rate; on some benchmarks, such as Dhrystone, it is as much as 35–40% faster. Typical power consumption is only 80 mA at 16 MHz with a 3.3-V supply. In standby mode, power consumption drops to 3 mA, and with the clock stopped, it is only 50 µA.

VMT's 386SX+ is offered in either an Intel-compatible PQFP or in a smaller TQFP that is only 1.5-mm thick and 16 mm on a side. The major target for the 386SX+ is not in PCs, for which the market window has passed, but in consumer electronics. (The chip is significantly slower than Cyrix's 486SLC, so it cannot compete in the notebook computer market.) VMT currently is marketing its chips only in the Far East.

VMT plans to use its 386SX+ core as part of highly integrated system chips for consumer electronics and handheld computer applications.

Contact V.M. Technology Corp. in Tsukuba, Japan at 0298.51.1982, fax 0298.51.0184.

more significant derivatives that will add system logic and other functions to the processor chip. The first such chip, code-named Rio Grande, is promised for delivery in the first half of next year.

An Integrated Future

It seems likely that TI's and Cyrix's paths will continue to diverge. Cyrix disclosed its M1 superscalar x86 implementation last month at the Microprocessor Forum *(see **071401.PDF**)*, and the following week a TI executive said that the company has its own design team working on a next-generation CPU.

In his presentation at the Microprocessor Forum, TI's Ian Chen described a hypothetical 1996 device, incorporating 3 to 4 million transistors, that includes a next-generation CPU with on-chip system logic and a DSP core, operating at voltages as low as 1.5 V and consuming only 0.5 W. The hypothetical design allocated 2 to 3 million transistors to the main CPU, 800,000 transistors to a DSP core, 200,000 transistors to video, and 500,000 transistors to system logic, a PCMCIA interface, a network interface, and other control logic.

TI plans to implement such devices using a modular design method that would allow quick customization, much like the one Motorola has pursued with its 68300 embedded processor family. TI naturally hopes to leverage its DSP strengths by including a DSP core, although it remains to be seen whether there will be a real demand for DSPs in PCs and whether it will be economical to integrate the DSP on the main CPU chip.

Filling Holes

TI's 486SXL2 joins Cyrix's 486S in attempting to fill one of the few notable gaps in Intel's product line: the lack of a 486SX2. Both the Cyrix and TI devices fall short of Intel's performance at the same clock rate due to the slightly slower core CPU design, and neither Cyrix nor TI can yet match the 66-MHz clock rate Intel has achieved for its 486DX2. Faced with Intel's aggressive pricing of its 486SX, Cyrix has stopped promoting its 486S. Although TI's 486SXL2 has a larger cache, matching Intel's, it isn't likely to fare much better than the Cyrix design.

A large 486SX2 market will emerge eventually, but it will be dominated by "full" 486SX2 devices from AMD and Intel. AMD is reported to have a 486SX2 ready, but it has not announced it. Today, Intel and AMD are production-limited, and the profit per wafer is much higher for a 486DX2 than it would be for a 486SX2. Next year, when both AMD and Intel move their 486 designs to 0.6-micron processes and more capacity comes on line, a 486SX2 from both companies will be more likely.

Intel could, of course, introduce a 486SX2 at any time should doing so prove to be important from a competitive viewpoint; only a trivial amount of engineering would be required (indeed, it is possible that existing 486SX chips have clock-doubling circuitry and that it is simply not enabled).

TI is likely to have its best success with the 486SXLC2, which is handicapped by its 16-bit bus but is better suited than the 486SXL2 to subnotebook systems because of its small package size and lower cost. It also allows system makers to easily extend the life of 386SX-based hardware designs, delivering superior performance for such systems and offering something that Intel and AMD don't.

While integration of system logic and other functions on the CPU chip has not, so far, proven to be particularly successful, Intel's termination of its SL integration strategy leaves this as a natural market for others to exploit. While such chips may not produce as much revenue per silicon area as Intel's high-end CPUs, they could still be very attractive when compared to other semiconductor products. This is therefore a natural path for TI to pursue, and it will also give TI continued differentiation from the Cyrix products.♦

