AMD Describes Enhanced 486

Version with 16K Write-Back Cache Aimed at Dual-CPU Systems

by Michael Slater

While not describing an actual product, AMD's Jim Bowles presented at last month's Microprocessor Forum the case for a 100-MHz 486 with a 16K write-back cache. The clock rate was forecast to reach 120 MHz in 1995.

This hypothetical product was described as enabling a dual-processor PC, in which the second processor could be added as an end-user upgrade. Intel is expected to pursue the same dual-processor strategy with a future revision of Pentium, code-named P54CM. Pentium already has a 16K cache, though it is split instruction/data rather than unified. Intel's planned multiprocessor extensions apparently consist primarily of adding its APIC interrupt controller to the processor to enable a glueless two-CPU system. AMD's design does not include interrupt logic, which can be provided externally.

Bowles estimated that doubling the on-chip cache to 16K would improve the hit rate by 5–10% and reduce bus activity by 7–15%. The write-back mode has an even bigger effect on bus utilization, cutting it from 70% to less than 40%.

Normally, 486 bus arbitration is implemented with HOLD and HLDA. Bowles described an alternative scheme using BOFF# (back-off) instead. This has the advantage of offering very low latency, reducing the amount of time each processor is stalled waiting for bus access; the processor will relinquish the bus in the next clock cycle, rather than waiting for the current instruction or even bus transaction to complete. It requires external logic to ensure that all bus operations, including locked transactions and cache-line fills, are handled properly when the bus is requested.

Bowles described the enhanced 486 as being used in a dual-processor configuration with a shared second-level cache, which is the same approach Intel is taking with its dual-processor Pentium design. Today, most multiprocessor systems provide a dedicated second-level cache for each CPU, which is essential if the system is to be scalable to more than two processors. For just two processors, however, the shared L2 cache may be acceptable, especially with the increased on-chip cache size.

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"No one has yet come up with a commercially viable SMP operating system…until Windows NT."
Jim Bowles, AMD

The key advantage of this approach is that, other than the cost of the processor chip itself, the additional cost of supporting a second processor is near zero. An upgradeable, uniprocessor system would carry no price premium, and would offer an OverDrive-type upgrade that would make it a dual-processor system. Since the incremental cost to the user for the second processor would probably be less than 20% of the system price, even a modest speed boost could justify the expense.

Windows NT, which includes MP support, could make dual-processor PCs appealing. A single-processor Pentium system will be more attractive to many users, however, because of its higher performance on single tasks. AMD implied that the enhanced 486 would cost less than half as much as a Pentium, which suggests that 486 pricing will drop dramatically by the time this chip is introduced. The Pentium system would have the advantage of still having an upgrade path to two processors.

There are situations in which running two applications, each on its own processor, has some benefit, but this is not enough to make a dual-processor system compelling for most users. Having two processors won't make a single application run faster unless that application is written as multiple threads. Windows NT and the forthcoming Chicago (i.e., Windows 4) will support multithreaded applications, and once applications evolve to support the capabilities of these operating systems, single-user, multiprocessor systems may become more popular.

While the dual-processor application is the most innovative, a 16K, write-back cache version of the 486 is likely to be most popular simply as a higher-performance replacement for the 486 in uniprocessor systems. Such a chip could be a powerful competitive weapon against Intel's 486 line, since it could offer higher performance in a pin-compatible device. The die size would inevitably be considerably larger, but the profit margins are sufficiently high that this would not keep AMD from pricing the chips competitively, should it choose to do so. Intel, of course, could also produce 16K cache, write-back 486 chips. Indeed, if AMD finds more production capacity and succeeds in bringing such a chip to market, Intel could be all but forced to respond in kind. ♦

