Sony & HDL Detail Embedded MIPS Cores

Custom vs. Synthesized R3000 Designs For Low Power And Cost

by Brian Case

At last month's Microprocessor Forum, both Sony and HDL Systems described MIPS processor cores designed for use in low-cost, low-power, customer-specific embedded chips. The most interesting difference between the two cores is that Sony's chip, the R3100, is a custom, hand-packed processor layout, tailored to the company's needs and technology. HDL, on the other hand, uses a high-level Verilog model and design synthesis to create logic and circuit designs and layouts tailored to specific customer needs and varying process technologies.

Embedded Means "Embedded In Silicon"

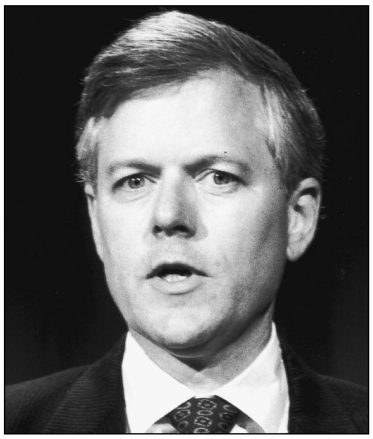
Normally, the term embedded indicates that a processor is used for a specific purpose in a system design and is essentially invisible to the system user. For Sony and HDL, however, embedded also means that their processor cores are combined with customer- and application-specific circuitry on a single chip. The day will come when the processor core is essentially invisible to the system designer who uses the chip.

Embedding processor cores into single-chip designs to reduce cost and size has been done for many years, but usually microcontroller-class cores have been used. Powerful 32-bit, general-purpose processors have historically been too big, power-hungry, and too hard to use to be cheap. Another important consideration has been the lack of support tools for 32-bit processors. The problem with low-performance, microcontroller-class processors is that they often require special logic—or even supplementary processors—to accelerate functions that need more performance than the processor core can deliver.

In the past couple of years, process technology has become dense enough and automatic design tools reliable enough to permit cost-effective use of MIPS and other high-performance processor cores in ASICs and CSICs. To some extent, VLSI has pioneered this market with its embeddable 32-bit ARM processor cores.

The major benefit of using a standard 32-bit processor core is performance. A high-performance processor core can typically handle compute-intensive functions that might have required a separate processor. Another benefit is the ability to use tested, high-quality design tools that have been developed for other uses, such as application development in the workstation market. A plus for many customers is the security associated with a standard processor core that is available from a variety of vendors.

The extent to which fast, 32-bit processor cores will enter new markets is evident from plans that Sony and HDL have for their designs. Sony sees opportunities in global-positioning systems (GPS), mini-disc consumer audio, modems, smart TV, MPEG-1 applications, and PDAs. Sony is known to be working with General Magic on a PDA application but says the R3100 project started long before the relationship with General Magic began.



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"Our cores are small and technology-independent, so they are embeddable in any type of silicon application."

Terry Smith, HDL Systems

HDL is encountering customer interest in PDAs, cable set-top boxes, multimedia audio boards for PCs, and fiber-channel interfaces. Most of these applications are of the high-volume, low-cost type that would have been considered out of the reach of expensive 32-bit processors just a couple of years ago.

The Sony and HDL designs are quite similar at the microarchitectural level and have many features in common because the target applications have similar requirements. At the same time, the cores are implemented with completely different approaches because the target audiences are different. Sony is its own customer, while HDL designed a core that could be modified according to the varying needs of different customers and a range of technologies.

HDL Offers Architectural Flexibility

HDL—a tiny, four-year-old design firm—has been a MIPS licensee for two years. In that time, the company has built and verified a Verilog model of the MIPS R3000 processor core. The company's core Verilog code has been used to build commercial simulation models of the IDT 3051 and 3081 embedded microprocessors; twelve companies are using the models. HDL points to the success of these models as proof that the correctness of their R3000 Verilog model is well validated.

About a year ago, HDL decided to change its business strategy from simulation models to chip design. The long-term goal is to sell chips into the application-specific market, but the short-term focus is customer-specific designs. The application-specific market has the advantage of a wider range of customers and therefore more reliable volumes, but the customer-specific market is the best way for HDL to leverage its unique capability.

What sets HDL apart in the customer-specific market is its chip design strategy. First, HDL has the ability to combine the high-level Verilog code for the processor core with Verilog code for the customer's peripheral logic into a single simulation model. Second, the Verilog code for the processor core can be modified to meet a customer's special requirements. Third, after the design is debugged through simulation, HDL uses Synopsys logic synthesis to produce a logic design from the model of the combined processor and customer logic. This logic design can then be targeted to a number of generic gate-array or standard-cell fabrication processes.

HDL says that the major selling points for its design approach have been the architectural flexibility provided by the high-level processor model and the technology independence provided by logic synthesis. Quick design turn-around is another advantage.

A design with HDL usually progresses through two phases. The first phase maps the Synopsys-generated logic design onto a standard sea-of-gates chip. This chip is used to get application software development started and provides a means for validating hardware. For the second phase, in high-volume designs, HDL is equipped to reimplement the design using an optimized standard-cell methodology, which can significantly lower chip cost.

For More Information

Contact Sony Semiconductor Component Products at 714.229.4464, fax 714.229.4271. Contact HDL Systems at 408.522.2600, fax 408.522.2626.

HDL Core Features

The HDL core design uses the basic five-stage MIPS R3000 pipeline: fetch, decode, execute, memory access, and write-back. The core is available in several versions that have the optional features shown in Figure 1.

The HDL core is distinguished from the basic R3000 core in several ways. First, power and space—40% of the area needed for a full-fledged R3000 core—are saved by eliminating the MMU. The TLB accounts for most of the area saved, but reduced routing and simplified control logic make a significant contribution as well. Even without the MMU, the HDL core retains the memory protection associated with the user/kernel processor mode distinction.

Small, direct-mapped 4K instruction and 1K data caches are typical in HDL's standard cores, but characteristics are programmable, which allows customization of total size and line size for specific needs. The caches can be removed for applications that do not require them.

Unlike standard R3000 caches, which use one tag per word in both caches, the HDL caches use one tag per eight instructions and one tag per four data words. HDL can build its cores with different cache line sizes to minimize tag-store size, which can be important in high-volume applications. HDL believes it is unique in offering this flexibility.

To accommodate interrupt-intensive designs and reduce response time, the HDL core implements vectored interrupts. The standard MIPS interrupt mechanism is to vector all interrupts to a single handler that examines a "cause" register to determine the interrupt source.

The HDL core has a set of bit-test instructions that is not present in the standard MIPS instruction set. While a single bit-test instruction can replace a sequence of three or four instructions, at first it seems unlikely that these instructions could make an HDL core usable where a standard R3000 would not be. According to HDL, however, when the fast bit test is combined with the vectored interrupts, the HDL core can handle some servo-motor control tasks in disk drives, for example, that previously required dedicated hardware.

The bit-test instructions will be useful only in hand-

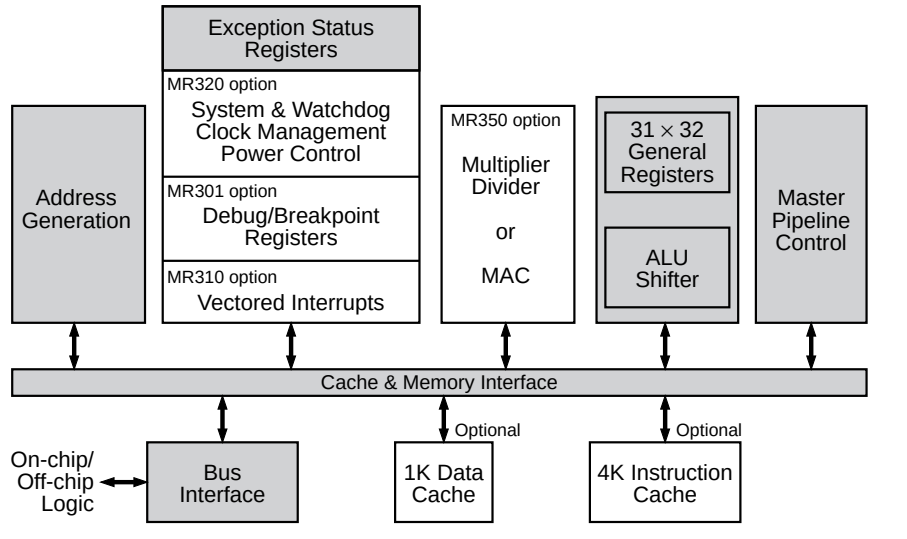

Figure 1. The HDL core is offered in several standard versions. The MR350, with the multiplier/divider or multiply-accumulate hardware, offers the highest performance for most applications.

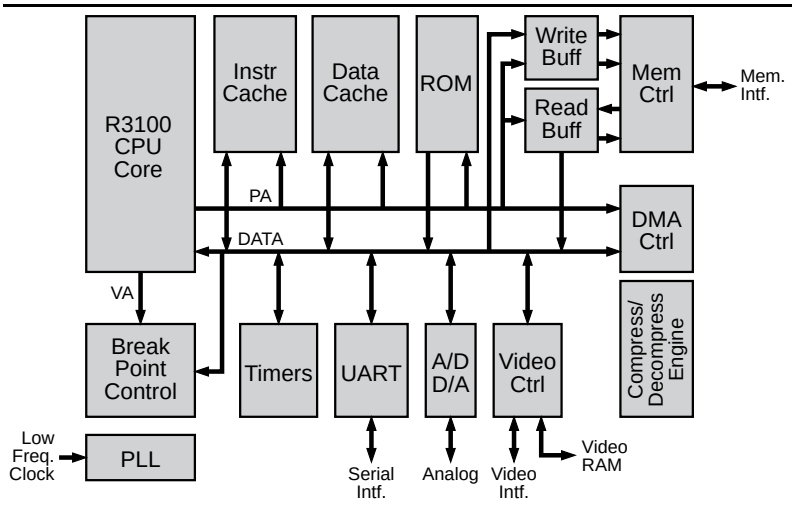

Figure 2. Block diagram of a typical R3100 single-chip system. The Sony core offers a digital phase-locked-loop for clock control, which permits the use of a low-frequency oscillator. This is important for consumer applications which must use low-cost shielding.

coded routines, like interrupt handlers, because standard compiler support is unlikely.

One of the most significant additions HDL made to its MIPS core is the multiply-accumulate capability. New instructions access the 64-bit accumulator, and extended instructions were added to write results to the register file. The MR350 core includes a 16 × 16-bit hardware multiplier to speed standard multiply instructions and the multiply-accumulate.

A 16 × 16 multiply-accumulate has a two-cycle latency with one-cycle throughput. A 32 × 32 multiply-accumulate has a five-cycle latency with four-cycle throughput. A faster, 32 × 32-bit hardware multiplier is being designed now and will speed the 32 × 32 multiply-accumulate to two-cycle latency, one-cycle throughput.

For many applications, power-saving techniques will be HDL's most significant additions to the MIPS core. The implementation is fully static, which allows the processor clock to be slowed or even stopped completely to save power when processing demands are low. Optional clock circuitry allows the input clock rate to be divided by powers of two (up to a diviser of 64) or stopped under software control.

Another significant power savings is achieved by removing power from the caches when they are not used. Of course, the instruction cache is accessed frequently, but the data cache is used only about 20% of the time in a typical instruction mix. It's easy for the cache control circuits to sense when to power-up the data cache because a load or store instruction in the decode stage of the pipeline gives at least two cycles of warning before the instruction reaches the memory stage.

Custom Design Meets Sony's Needs

To design a MIPS core for internal use, a group of Sony design engineers in the US teamed with a group of circuit-design specialists in Japan. The goal was a standard MIPS processor core suitable for use in Sony's mainstream consumer-electronics products. As with the HDL design, the Sony core had to deliver high performance with a small die size (i.e., low cost) and low power consumption.

The engineers began by designing a completely compatible R3000A MIPS chip. As with the HDL design, only the high-level architectural models from MTI were used; the MTI-supplied mask-level design was not. They proved their design correct by replacing the processor chip in a commercial R3000A-based MIPS workstation with their own chip.

The major advantage of this approach is that the engineers have deep, intimate knowledge of the design from top to bottom. The teams can use this knowledge to produce optimized derivative designs. In contrast, modifying the mask set to produce a new chip limits the ability of the design team to make modifications efficiently.

For Sony, the extra expense and time needed to arrive at a fully custom design is justified by the economics of its business. In a low-cost, high-volume consumer product, saving even a few pennies in die cost can be well worth the effort.

While this processor core is primarily for internal use, Sony leaves open the possibility of licensing it as an embedded core in the near future.

Sony did say, however, that it would license the core if a large customer sought a partnership and was willing to live with a lack of traditional, formal support. Further, if the projected volume is high enough, Sony might even agree to customize the core.

Sony Core Features

Because they are aimed at similar applications with similar requirements, the Sony and HDL cores share many characteristics. There are, however, a few significant differences. Figure 2 shows a block diagram of a typical chip using the Sony R3100 processor core. Sony started with the design database proven via the R3000A chip and, like HDL, removed the MMU and added multiply-accumulate and debug facilities.

As HDL did in its core, Sony implemented the standard five-stage R3000 pipeline. Cache sizes are the same, 1K data and 4K instruction, and both are direct mapped. Line sizes are much smaller, however, with the data cache at a four-byte line and the instruction cache at a 16-byte line. Sony designed the instruction cache to be a factor of four times the data cache in both overall size and line size so that the same tag structure could be used for both caches.

The multiply-accumulate facility is similar to the one offered by HDL. The multiplication produces a 32-bit result, but the accumulator is a full 64 bits wide. While this uses more hardware, Sony says that at least a 48-bit accumulator is required in modem applications, so it seemed only natural to simply build a double-precision accumulator.

The multiply-accumulate instruction can perform a 16-bit multiply and 64-bit accumulate in one clock. A full 32-bit multiply-accumulate requires four clocks. The multiplier also speeds up the regular MIPS multiply instructions. If the upper 16 bits of the operands are simply sign-extension bits, a regular multiply instruction will complete in one cycle; otherwise, five cycles are required. This compares favorably to the 12-cycle multiply time for standard R3000 implementations.

MICHAEL MUSTACCHI

"We would like to make MIPS processors the Z80 of the future."
Tuan Luong, Sony America

Power control in the current version is similar to that offered in HDL's design. The Sony core is fully static, so the clock can be stopped to reduce power consumption to a minimum. As in the HDL design, the cache sense amplifiers are powered up only when a cache access is actually needed.

In the next version of the core, Sony will be more aggressive with power control. Logic blocks, such as the multiplier, that consume a lot of power but are not always used will not be clocked when they are idle.

Unlike HDL, Sony uses a digital PLL for clock control so a low-frequency external oscillator can be used. This is extremely important for consumer products, which must meet EMI standards with inexpensive system shielding. The designers were told to expect an external system clock rate of no more than 10 MHz. Like the clock circuitry in the HDL core, the PLL is able to produce a variety of internal clock speeds to regulate power consumption.

A digital PLL was used instead of an analog PLL to allow Sony to easily implement the core in different IC process technologies, but it is difficult to achieve a 50% duty cycle with a digital PLL. The logic and circuit design had to be adjusted for a non-50% duty cycle.

Technology Comparison

The Sony core is currently implemented in a 0.5-micron, two-layer-metal CMOS process. The core without caches requires 16 mm^2 of die area; with caches, the die area swells to 36 mm^2. The CPU core alone requires about 180,000 transistors or about 480,000 with cache.

The maximum on-chip clock rate for Sony's fully static design is 40 MHz. Although this seems slow by the standards of workstation microprocessors, it is at the high end of the range for embedded processors. R3100 power consumption is rated at 25 mW/MHz with a 3-V power supply. At 40 MHz, a full watt of power would be dissipated, so intelligent power management will be required in battery-powered applications.

The statistics for the HDL core, of course, depend on the fabrication technology used by HDL or its customer. It makes sense, though, that most will choose a silicon vendor that HDL has used before, to minimize possible snags in the development process.

HDL is working with two Japanese chip vendors to implement its designs. One is making a sea-of-gates version, the other a standard-cell implementation. The standard-cell version of the MR300 core in a 0.6-micron, three-layer-metal CMOS process is just under 9 mm^2 (not including cache or MAC hardware). This compares favorably with the 6-mm^2 ARM700 core *(see **071503.PDF**)*. HDL says hand-packing portions of the core will reduce area even further.

HDL claims to have achieved 33-MHz operation for a 3-V version of its core and is currently designing a 40- MHz, 3-V chip for delivery in 1H94. The speed boost will come from designing special standard cells and layout optimizations. Specific power-consumption data is not yet available.

The difference between the sizes of the HDL and Sony cores can be partly explained by process technology—two vs. three metal layers—and partly by the fact that the HDL core for which the size is quoted does not include the multiply-accumulate or debug circuits.

Significant Market Impact Expected

Sony and HDL have designed MIPS cores that can bring new levels of performance to a variety of consumer-electronics products. One of the challenges for this market is making the devices truly appealing to non-technical users. Usually, this means providing natural input and output capabilities, such as audio, that create or require essentially analog data streams.

The high clock rates, caches, and multiply-accumulate instructions in these processor cores will allow natural input and output to be incorporated into many devices without the use of a separate DSP. This will either allow devices to be built that would otherwise have been too expensive or to simply reduce the cost of existing devices. Sony, for example, may be able to eliminate the hardware compression/decompression circuits currently used in its mini-disc consumer audio products. By combining 32-bit performance with low cost, both MIPS cores will be appealing in many new consumer applications.♦

