

## Literature Watch

## Buses

**IC passes 350 Mb/s through ring architecture.** The QR0001 provides high-speed interconnect that is ideal for high-speed streams of data, such as digital video. Richard Nass, *Electronic Design*, 10/1/93, p. 127, 2 pp.

## Development Tools

**Programmable logic helps speed ASIC development.** Three easy-to-follow rules for producing digital circuits that translate into fully-functional and reliable ASICs. Jerry Machado, *Electronic Design*, 10/1/93, p. 26, 7 pp.

**SBus emulator debuts TI DSP devices.** SBus-based emulator lets SPARCstation-compatible platforms develop and debug systems based on TI TMS320Cx and TMS320C40 processors. Tom Williams, *Computer Design*, 10/93, p. 118, 2 pp.

**HDLs extend logic-design methods, not replace them.** Making the transition from drawing circuits to describing them using Verilog HDL. Randy Crane, Hewlett Packard; *EDN*, 10/14/93, p. 111, 6 pp.

**Logic Scope simplifies digital circuit debug.** One instrument comprises a high-performance DSO and a logic analyzer with cross-triggering capability. John Novellino, *Electronic Design*, 9/16/93, p. 135, 2 pp.

**Tool vendors poised to meet EMI challenge.** EMC Advisor software is an expert system tool that guides PCB layout and routing. Mike Donlin, *Computer Design*, 10/93, p. 46, 2 pp.

## DSPs

**IC aims at digital-audio decompression standards.** Complete audio subsystem on a chip integrates DSP core, programmable phase-locked-loop, clock multiplier, and stereo DAC circuits. Jack Shandle, *Electronic Design*, 10/1/93, p. 45, 4 pp.

**Codec compresses images in real time.** C-Cube's CL4000 can perform real-time MPEG encoding and decoding for full-motion video applications. Dave Bursky, *Electronic Design*, 10/1/93, p. 123, 2 pp.

**Multiprocessing exploits DSP performance potential.** Multiple DSPs on a single board eliminates overhead, improving performance and flexibility. Tony Agnello, Ariel; *Electronic Design*, 10/1/93, p. 50, 6 pp.

## Graphics

**Introduction to the Computer Graphics Reference Model.** The basic framework for defining standards for graphics, such as transmitting, compressing, and rendering images. George S. Carson, *Computer Graphics*, 9/93, p. 108, 12 pp.

## Memory

**Flash memory goes mainstream.** With its high-density, non-volatility, and production volumes, flash RAM is the first significant change in solid-state memory in a decade. Brian Dipert, Lou Hebert, Intel; *IEEE Spectrum*, 10/93, p. 48, 5 pp.

## Miscellaneous

**Protecting industrial property rights.** Using modeling techniques to compare patents vs. copyrights as protection for intellectual property. Richard H. Stern, Graham & James; *IEEE Micro*, 10/93, p. 2, 6 pp.

**Should you take the leap? Raw CPU performance is important, but balancing CPU and I/O speeds is essential for a cost-effective solution.** Allen G. Taylor, *Computer Power*; *UnixWorld*, 11/93, p. 56, 3 pp.

**The soul of a new OS.** Support for multiple personalities and distribution of services across platforms makes systems flexible and resilient. Rik Farrow, *UnixWorld*, 11/93, p. 62, 3 pp.

**High-speed networking chips stalk the desktop.** Emerging network standards FDDI, ATM, and Ethernet offer to bring 100+ Mbps network speeds to the desktop. Jeff Child, *Computer Design*, 10/93, p. 57, 6 pp.

## Processors

**The Gmicro/500 superscalar microprocessor with branch buffers.** A significant advance for the TRON architecture. Kunio Uchiyama, et al, Hitachi; *IEEE Micro*, 10/93, p. 12, 10 pp.

**The  $\mu$ VP 64-bit vector coprocessor: a new implementation of high-performance numerical computation.** Designed specifically for high-speed numeric operations, the  $\mu$ VP achieves 206-Mflops at 50 MHz. Makoto Awaga, Hiromasa Takahashi, Fujitsu; *IEEE Micro*, 10/93, p. 24, 11 pp.

**Fuzzy inference and fuzzy inference processor.** For demanding high-speed control applications, this hardware solution to the fuzzy inference problem reaches 200K inferences per second. Kazuo Nakamura, et al, Mitsubishi Electric; *IEEE Micro*, 10/93, p. 37, 11 pp.

**The PowerPC 601 microprocessor.** Combining IBM's POWER architecture with Motorola's bus structure brings a powerful, competitive processor to market quickly. Michael C. Becker, Motorola, et al; *IEEE Micro*, 10/93, p. 54, 15 pp.

**New versions of 386 spell relief for embedded designers.** Jeff Child, *Computer Design*, 10/93, p. 42, 3 pp.

## Programmable Logic

**32-bit embedded designs need a new approach.** John Sambrook, Jess L. Thompson, Applied Microsystems; *Electronic Design*, 10/1/93, p. 12, 6 pp.

## System Design

**How does processor MHz relate to end-user performance? Part 2: memory subsystem and instruction set.** The importance of the memory subsystem when comparing superscalar and high-clock-speed processors. Steven W. White, IBM, et al; *IEEE Micro*, 10/93, p. 79, 11 pp.

**Aim 32-bit power at embedded-control designs.** John T. Burns, Fujitsu; *Electronic Design*, 10/1/93, p. 42, 5 pp.

**Control clock skew with intelligent distribution.** Tim Thompson, Applied Micro Circuits; *Electronic Design*, 10/1/93, p. 56, 6 pp.

**Recent advances stretch Bipolar/BiCMOs processes.** Frank Goodenough, *Electronic Design*, 9/16/93, p. 73, 5 pp.