Most Significant Bits

AMD Extends 486 Line

Advanced Micro Devices has announced two new 486 processors. The company officially released its 66-MHz 486DX2, a speed discussed when AMD first announced its 486 chips *(see **070601.PDF**)*. The new version allows AMD to match Intel's current high-end 486 products, although Intel is expected to announce faster 486 chips by the end of the year. AMD's 66-MHz part is priced at $463 in 1,000-piece lots, the same as Intel's 4Q93 pricing; given the current undersupply of 486 chips, AMD has no reason to compete on price.

AMD's second new chip, the 486DXL, is a 5-V version of the previously announced 486DXLV. It is similar to Intel's SL-Enhanced 486s in that it adds system-management mode (SMM) to the base 486DX design. The DXLV is currently available only at 33 MHz; by raising the voltage, the DXL will ship at 40 MHz. At that speed, the price will be $283, matching the price of Intel's 33-MHz 486DX. (Intel does not market a 40-MHz 486DX.) Both new processors are sampling now with volume shipments expected by the end of the year. AMD expects to eventually offer SMM on all its 486 chips, matching Intel's SL-Enhanced strategy.

In a shrewd marketing move, AMD also announced a licensing agreement with Microsoft that will let it brand its chips as Windows-compatible. This move shifts the argument from whether AMD's chips are compatible with Intel's to the more important question of whether they are compatible with the huge base of PC software, leveling the playing field for all processor vendors. Other x86 chip vendors are likely to adopt the same branding, although Intel will probably stick with its well-funded "Intel Inside" campaign.

VLSI Announces Fuzzy Processor

At last month's Microprocessor Forum, VLSI Technology announced a 12-bit fuzzy logic coprocessor for embedded applications, the VY86C570. By performing fuzzy calculations in hardware, the new chip is an order of magnitude faster than a traditional microcontroller running software-based algorithms: it can perform more than 850,000 rule evaluations per second running at 20 MHz. The '570 also includes on-chip rule-base memory to reduce system costs.

Fuzzy logic deals with imprecise values rather than binary logic and can be used to quickly solve problems that are unwieldy or unsolvable using traditional approaches (see MPR 2/20/91, p. 11 for more details). Fuzzy systems process inputs based on a set of rules to produce one or more outputs. While the inputs and outputs are "crisp" (non-fuzzy), the internal evaluation is done using fuzzy variables.

The '570 was jointly developed by VLSI and Togai InfraLogic. The fuzzy core processor itself, which VLSI calls the 86C500, is based on Togai's FC110 design *(see **061702.PDF**)*. The '570 also includes 4K words (12 bits per word) of on-chip memory for the rule base, 256 words of on-chip memory for temporary storage, an external memory interface, and a host bus interface. Typically, the fuzzy coprocessor is connected through the host bus to the main processor, which uses the temporary storage to download input values and read output values from the coprocessor.

The on-chip rule memory is sufficient for many fuzzy applications. For example, it can contain up to 750 rules for a simple two-input, one-output system or up to 170 rules for a more complex system with 20 inputs and eight outputs. For very complex systems, the '570 supports up to 64K words of external rule memory.

Togai's TILShell development environment supports the '570. The new chip uses a 68-pin PLCC. It is currently sampling, with volume shipments expected in 1Q94. Pricing is set at $40 in 1,000-unit quantities.

Fuzzy logic has become quite popular recently. Most designers today are using software-based solutions, but the performance of the VLSI chip will be attractive to those users who are attacking more complex problems. There are few other fuzzy logic processors on the market; Togai's own implementation of the FC110, for example, is about the same price as the '570 but is slower and has no on-chip rule memory. Thus, the VLSI processor could do well in this fledgling market for those applications that require its high performance.

Motorola Expands 68300 Family

Motorola has introduced the 68307, the first 68000-based member of its integrated 68300 family with a static design. It combines a 16-bit 68000 core with a variety of peripherals and bus interfaces, and power management. The new chip, which can operate at 3.3 V, is aimed at portable applications such as digital cordless telephones. These applications typically require lower cost and lower performance than Motorola's 6834x parts *(see **070804.PDF**)*.

Like other 68300 parts, the '307 includes a basic set of system functions, such as two 16-bit timers, two 8-bit parallel ports, and one serial port. Another port interfaces with the I^2C protocol used by some ROM and peripheral chips. There is no on-chip DRAM controller; Motorola assumes that most designs using the '307 will have static memory.

The '307 includes an unusual bus interface that can be configured to operate with either standard 68000 or 8051-style protocols. This allows the reuse of ASICs and

peripheral chips designed for these two common buses.

The new chip consumes minimal power, extending battery life. The 5-V, 16-MHz part requires a maximum of 150 mW. The 68307V is a 3.3-V version that uses just 40 mW when operating at its peak rate of 8 MHz. Both chips consume less than 1 mW when the clock is stopped.

The 68307 and '307V are both packaged in 100-pin PQFPs and priced at $11.29 in 10,000-unit quantities. These parts are expected to sample in 1Q94, with production in 2Q94. The company expects to produce a 16-MHz '307V one quarter later, at a price of $12.80.

Motorola reports that the '307 was designed in just three engineer-months by combining existing standard-cell building blocks to a customer's specification. This capability allows the company to respond quickly to changing market needs. This is similar to the strategy that AMD is proposing for its Customer-Specific Products Division (see ***0709MSB.PDF***). Motorola, however, has already demonstrated its mastery of this technique.

IIT Puts Video Conferencing on a Chip

Integrated Information Technology has combined its Vision Controller and Vision Processor (see MPR 10/30/91, p. 1) into a single chip, the VCP. In addition to the functions of the Vision chip set, the new chip also includes split video ports, a new audio port, and additional hardware capabilities to improve performance. With the addition of some memory and an external DSP, the VCP creates a complete two-way teleconferencing interface with H.261 (px64) video at CIF (352 × 288) resolution and H.320-compatible audio.

The 0.8-micron CMOS chip operates at speeds up to 66 MHz and is expected to sample in 1Q94. Later next year, a 0.65-micron version running at 80 MHz will be able to decode MPEG-2. Volume pricing ranges from $140 for a 20-MHz version to $400 for the fastest parts.

Cray Announces Alpha, SPARC Systems

Cray Research has announced its first Alpha-based system, a massively-parallel processing (MPP) product dubbed the T3D. As hinted by the name, the system uses a three-dimensional interconnect model. Each node consists of two 150-MHz 21064 processors, each with 16M or 64M of local memory. A node contains a fast switch that connects to six other nodes, two each in the X, Y, and Z axes. Each node has a peak communications bandwidth of 2.1 Gbytes/s; the nodes are connected in a three-dimensional torus, reducing the maximum message-passing latency in large configurations.

The system uses a multiple-instruction, multiple-data (MIMD) programming model. The base system, including 32 processors and 512M of memory, is priced at $5.5 million; this price includes a built-in Cray Y-MP processor that is needed as a front end for the T3D. Configurations of up to 2048 processors are available, but liquid cooling is required for systems with more than 128 processors. Cray rates the peak performance of the 1024-processor system at more than 150 GFLOPS, based on the 150-peak-MFLOP rating of the 21064.

Cray Research also announced extensions to the SPARC product line that it inherited in its acquisition of Floating Point Systems (FPS). The new CS6400 combines 4 to 64 SuperSPARC processors. It is the first announced system to use 60-MHz SuperSPARC chips. The CS6400 will run Solaris, making it compatible with most Sun systems. In fact, Sun has agreed to resell the new server. List pricing ranges from $400,000 for a four-processor system to $2.5 million for a 64-CPU box.

These announcements show that general-purpose RISC microprocessors are beginning to penetrate even the highest-performance segments of the market. Cray Research has realized that it is most effective in building the high-speed infrastructure needed for such large systems; rather than waste time designing a fast CPU, it simply bought the fastest one on the market. (Seymour Cray, now at Cray Supercomputer, stubbornly refuses to accept this idea.)

While the performance of these new systems is impressive, the design wins are unlikely to bring much financial gain to Digital or Sun. The size of the supercomputer market is so small that Cray Research is excited to have received nine orders for the T3D so far. The market is so small that the company conveniently provides a list of its supercomputer customers—all 202 of them. It's so small that Cray dreams of selling "hundreds" of CS6400 systems. The market is so small that…well, you get the idea. One positive: the announcements allow Digital and Sun to argue with IBM about who has the most "scalable" RISC architecture.

Fujitsu to Absorb HaL

Sources indicate that Fujitsu has acquired all outstanding shares of HaL Computer, giving it 100% ownership of the floundering company. Although HaL is privately held, Fujitsu recently purchased all shares held by employees for approximately $3 per share. Ex-employees (of which there are many) also benefited; former CEO Andy Heller *(see **0710MSB.PDF**)* sold three million shares.

HaL is developing a 64-bit processor implementing SPARC version 9. Due partly to Heller's reputation as one of the creators of IBM's first POWER processor, many expected the HaL CPU to deliver leadership performance. The processor, originally expected to debut in systems this year, has been beset by delays.

The company is now out of cash and needs the infusion of resources from Fujitsu to complete the project. At this point, systems are not expected to appear until late 1994 and probably will not meet their original aggressive performance goals. Thus, it is questionable whether Fujitsu will be able to recoup its latest investment. ♦

