MICROPROCESSOR REPORT

THE INSIDERS' GUIDE TO MICROPROCESSOR HARDWARE

VOLUME 7 NUMBER 17 DECEMBER 27, 1993

Alpha Maintains Performance Lead in 1993

PowerPC Winning Marketing Battle; Others Strive to Keep Pace

by Linley Gwennap

*At this time of year, we look back on the previous 12 months and forward at the year to come. Our coverage includes stories on general-purpose RISC chips (this article) and embedded processors (see **071703.PDF**). Our next issue will cover x86 chips and processors for PDAs. Happy New Year!*

The past year has seen the introductions of Windows NT and Pentium, two external events that shaped the RISC processor market as much as any announcements made by the processor vendors themselves. Most RISC vendors spent 1993 delivering the processors that they had announced in 1992; Digital's 21064A was the only new mainline processor revealed in the past 12 months, and even that chip is only a minor revision of the landmark 21064 design.

Most of the new RISC processors announced in 1993 focused on one of two specialty areas. With NT actually shipping, vendors aimed at PC price points with processors such as the R4200, R4600, 21066, 603, and microSPARC-2. These chips all strive to match Pentium's performance at much lower prices. At the other extreme were two expensive, high-performance processors for the scientific market: SGI's TFP and IBM's Power2.

Many vendors also scrambled to make their processors more attractive to third-party system vendors. To compete with the standard system-logic chip sets available for Pentium, vendors announced similar chip sets for MIPS, Alpha, and PowerPC processors, all of which connect to standard PC buses and peripherals. MIPS Technologies (MTI), Sun, and IBM all created new organizations to distribute design kits for their chips.

To commemorate the best and worst of 1993, we present our second annual "RISCie" awards.

Top Gun Flies Again

Last year, Digital's 21064 captured the performance award with an asterisk, since the fastest 21064 chips were shipping only in low-volume servers and were not available on the open market. During the past year, Digital has shrunk the chip to a 0.68-micron process, significantly increasing yield at the higher frequencies and allowing the company to deliver 200-MHz chips to anyone who wants them. With the help of some compiler enhancements, the 21064 is a repeat winner as the **World's Fastest Microprocessor**. As shown in Table 1 (see below), the Digital chip just edges out IBM's Power2 based on SPECint92.

The company shows signs of extending its lead in 1994 with its 275-MHz 21064A, which takes the award as the **World's Fastest Vaporware**. Digital expects the 21064A to hit 170 SPECint92 and nearly 300 SPECfp92 when it ultimately begins shipping around 3Q94. That should suffice for Alpha customers until the company can begin shipping its next-generation 21164 processor, slated for early 1995.

Digital took several steps to broaden the appeal of its RISC architecture. The company is selling design kits for the 21064 for a nominal $50 fee and is developing PCI-based system-logic chip sets for that CPU. Mitsubishi signed up to second-source Alpha chips but won't begin shipping for another year or so. Digital even said it is developing Alpha CPUs for handheld devices, taking the award for **Biggest Stretch of the Imagination**.

Perhaps the most significant announcement for Digital was the new 21066 processor, which brings Alpha to low-cost system designs by integrating memory and bus interfaces. In fact, the 21066 is the **First CPU to Integrate PCI** on the chip. Although Digital has not yet announced a 21066-based system, Carrera Computer (Laguna Hills, Calif.) is selling a monitorless system for less than $4,000.

Several small PC vendors have signed up to market Alpha motherboards and systems for Windows NT users, but so far, the top-tier vendors have eluded Digital. While the company has made major progress in the past year, establishing Alpha as the highest-performance processor for NT or UNIX, it needs to build a base of soft-

ware applications to achieve significant volume, particularly for NT. Signing a high-volume PC vendor would significantly boost Alpha's prospects.

The Empire Strikes Back

IBM's RISC chips also had a good year in 1993, which saw shipments of the first PowerPC system and the announcement of the 603, the first PowerPC chip developed by IBM and Motorola from scratch. This activity was overshadowed by the RISC industry's **Biggest Advertising Budget**. The two companies spent much of the year convincing the media that PowerPC is the top contender against the dominance of the x86. As Andre Agassi points out, image is everything, particularly with only one system in production.

IBM announced an open specification for third-party vendors to build PowerPC systems that will run Windows NT, Workplace OS/2, AIX, Solaris, Taligent, and maybe even the Macintosh OS—if Apple decides to license it. This new Prep platform *(see **071704.PDF**)* gives PowerPC the hotly contested award for **Most Operating Systems Supported** by a RISC CPU; IBM could extend its lead if, as rumored, the company ports its proprietary OS/400 and MVS environments to PowerPC.

The new IBM Power Personal Systems group will build and market these Prep systems, using IBM's powerful PC sales channels. The new IBM Microelectronics unit will market boards and components for these systems, including PowerPC processors and a PCI system-logic chip set. The Microelectronics unit will also market design kits for less than $5,000.

The 603 announcement demonstrates the potential of the PowerPC architecture to deliver significantly better price/performance than the x86. The 603 die is roughly the size of a 486 and probably half the size of the P54C, a cost-reduced version of Pentium that is due at about the same time. Yet the PowerPC chip, at speeds up to 80 MHz, will offer performance comparable to that of Pentium (or P54C) at the same clock rate. With such a difference in die size, the 603 could be priced substantially less than the P54C, although the Intel chip may ultimately reach higher clock speeds.

IBM and Motorola plan to continue rolling out new parts in the coming year, aiming to boost the performance of PowerPC to match the RISC leaders. In the next few months, we should see the introduction of the PowerPC 604, which IBM expects to run at 100 MHz and deliver 130 SPECint92. Late in 1994, the even-faster 620 is expected to debut at 150 MHz, exceeding 200 integer SPECmarks. The 604 is expected to ship in volume by 4Q94, with the 620 reaching that milestone in 1Q95.

Meanwhile, on the workstation side of the house, IBM revealed the Power2 processor, its first new CPU design in four years. The six-issue design takes the award for **Most Superscalar Processor** and, with its three-chip implementation and costly MCM packaging,

System	DEC 7000 Model 610	RS/6000 Model 990	Siemens RM540	HP 9000 Model G60	Sun prototype	Siemens PCE-5S/66	RS/6000 Model 250	Sun prototype
Processor	DECchip 21064	IBM Power2	MIPS R4400SC	HP PA7100	TI SuperSPARC	Intel Pentium	PowerPC 601	Fujitsu MS-2
Clock Rate	200 MHz	71.5 MHz	150 MHz	96 MHz	60 MHz	66.7 MHz	66.7 MHz	85 MHz
Cache (on/off-chip)	16K/4M	32K/256K	32K/4M	none/2M	36K/1M	16K/256K	32K/none	24K/none
espresso	125.4	93.8	80.8	89.7	69.5	62.5	58.4	57.0
li	111.5	130.7	107.6	83.2	77.3	88.8	74.2	60.2
eqntott	203.7	164.2	129.4	97.3	127.0	60.1	76.9	125.0
compress	85.8	112.6	64.3	80.5	42.1	42.9	41.2	37.6
sc	254.5	172.2	136.4	73.4	115.9	102.0	85.2	71.2
gcc	87.6	102.4	78.3	70.5	62.2	64.2	51.6	43.7
SPECint92	132.7	126.0	95.8	82.0	76.9	67.4	62.6	60.8
spice	100.2	138.4	80.0	121.5	66.4	51.6	43.4	41.3
doduc	131.0	148.8	83.8	138.8	96.8	52.1	56.4	45.8
mdljdp2	153.1	195.3	133.8	186.6	103.1	65.0	85.7	63.3
wave5	115.3	159.5	81.1	112.5	68.4	41.5	48.6	33.8
tomcatv	304.6	473.2	160.6	145.6	86.9	73.6	94.3	61.3
ora	156.2	195.3	111.2	263.1	191.1	64.1	61.1	81.0
alvinn	436.9	801.0	116.0	178.0	209.3	122.3	160.9	97.6
ear	587.6	516.2	210.9	251.5	113.3	160.0	143.8	72.3
mdljsp2	75.1	88.6	66.5	89.8	50.3	30.2	47.6	34.9
swm256	226.8	242.4	68.5	81.8	49.5	42.6	63.9	35.4
su2cor	291.9	481.3	115.7	302.8	136.0	49.4	72.6	58.4
hydro2d	216.8	235.8	117.3	249.5	93.7	57.6	53.6	41.1
nasa7	280.5	370.9	124.9	243.5	110.6	52.7	72.1	61.8
fpppp	193.3	297.7	82.4	237.1	121.3	85.7	89.7	52.9
SPECfp92	200.1	260.4	105.2	171.8	98.1	61.5	72.2	53.0

Table 1. Among shipping processors, Digital's 21064 is the leader in integer performance, but IBM's Power2 leads for floating-point applications. RISC chips such as microSPARC-2 and the PowerPC 601 deliver near-Pentium performance at a lower price. (Source: SPEC)

finishes a close second to MTI's TFP in manufacturing cost. The complex design delivers the **Best FP Performance** of any shipping microprocessor and beats all except the 200-MHz 21064 in integer performance.

Great Taste or Less Filling?

Speaking of TFP, the MIPS processor appeared in a January announcement but now is not expected to ship until next spring, making it an early contender for next year's award for Longest Time as Vaporware. As shown in Table 2, the pair of monstrous 298-mm^2 dice is also the **Most Expensive Processor** to manufacture, with an estimated cost of $1,010 according to our MPR Cost Model *(see **071004.PDF**)*. But the four-way superscalar CPU really cooks, with an external-cache bandwidth of 1.2 Gbytes/s and an estimated SPECfp92 rating of more than 200. SGI promises to give us some measured performance numbers "real soon now."

While a few scientists will get their kicks from TFP, the real action for MIPS vendors is at the low end of the market. Not one, but two low-cost MIPS processors debuted in 1993. As shown in Table 3, the R4200 takes the award for **Lowest List Price** at just $80 in volumes of 1,000. Despite its low price, the chip is expected to match the performance of a 60-MHz Pentium on integer code (read: Windows NT). Like TFP, the R4200 is expected to begin shipping next spring, but MTI has yet to reveal measured performance numbers.

At 77 mm^2, IDT's R4600 chip (née Orion) squeezes in as the **Smallest RISC Processor**. (PDA processors are not included in this category.) The R4600 die is slightly smaller than the R4200, but at its initial 100-MHz speed grade, the R4600 delivers about 20% more performance. Although IDT has not yet announced faster parts, system vendor Deskstation says it will begin shipping 133-MHz R4600 boxes in 1Q94. At this speed, the R4600 approaches the performance of the 150-MHz R4400, the current high end of the MIPS line.

After announcing the R4400 over a year ago, the various MIPS chip vendors struggled to produce the chip, which uses a 0.6-micron, three-layer-metal CMOS process with gate oxides about 90 angstroms thick (or thin, in this case). IDT was the first to master this tricky process, beginning volume shipments of 150-MHz parts in July; NEC and Toshiba have only recently reached this milestone, but Toshiba is now aggressively pricing its parts, with the fastest R4400SC selling for $860.

MTI demonstrated a 200-MHz R4400 at Comdex and expects this part to reach production by mid-1994, providing a midlife kicker until the next-generation T5 processor begins shipping in early 1995.

Little Shop of Processors

Sun spent much of the year unveiling plans to broaden the SPARC market and improve the competitiveness of its processors. The company disclosed a multi-year roadmap with ever-increasing performance; its prescription for matching other RISC vendors is called UltraSPARC, a next-generation processor due to begin shipping in (you guessed it) early 1995. Until then, the company will rely on its SuperSPARC and microSPARC lines to continue as the **Best-Selling RISC Chips** for general-purpose systems.

While last year SPARC was judged Wide of the Mark, this year it receives the rarely seen **Ahead of Schedule** award. Sun's roadmap originally showed SuperSPARC reaching 60 MHz by 1Q94, but TI seems to have overcome its initial fabrication and timing problems and announced 60-MHz shipments in July. This impressive accomplishment may have influenced Sun to select TI to build the high-end UltraSPARC processor. TI continues to overprice SuperSPARC, however, listing it at $999 plus $399 for the required cache-control chip, a total of about $1,400 for what remains the **Slowest High-End RISC Processor** at 77 SPECint92.

Sun, of course, pays much less but is still concerned about cost. The company has not yet announced systems using the 60-MHz SuperSPARC (although other vendors have). According to *Unigram.X*, TI is modifying SuperSPARC to include the synchronization logic needed to connect a 50- or 60-MHz CPU to a 40-MHz MBus; this logic is currently in the cache-control chip. This change would allow much less expensive systems at these frequencies; SuperSPARC's large on-chip caches should keep the performance loss to around 10–15%. Neither Sun nor TI would confirm this story, but it could explain the delay in Sun's introduction of 60-MHz systems.

At the low end of the market, Sun is a repeat winner of the **Biggest Little Microprocessor** award, this time for microSPARC-2. MS-2 is Sun's recently announced low-end processor but weighs in at 233 mm^2, even using Fujitsu's 0.5-micron process. The MPR Cost Model pegs the processor at about $195 to build, pretty steep for a chip that doesn't even outrun a Pentium.

HaL Computer, a Fujitsu subsidiary, had a rough year, as its long-awaited 64-bit SPARC processor failed

MicroSPARC-2 Hits 85 MHz

Sun Technology Business (STB) has added a new speed grade for its forthcoming microSPARC-2 processor. STB initially said that the part would debut at 70 MHz, but initial fabrication runs have demonstrated better-than-expected yield at higher frequencies. Both the 70- and 85-MHz parts are expected to begin shipping in volume in 1Q94, with 100-MHz parts later in the year. MicroSPARC-2 is manufactured by Fujitsu and marketed by both Fujitsu and STB; neither company has announced volume pricing for the chip.

to materialize. Founder and CEO Andy Heller led an exodus of employees, but the company pledges to ship products in 1994. Maybe it will, but for now we are giving HaL the **Waiting for Godot** award.

Ross Technologies began the year as a unit of Cypress and later was sold to SPARC-collector Fujitsu. In the meantime, the company managed to finish its hyperSPARC design and begin shipments in 3Q93, 15 months after the initial announcement, coming in second for the **Longest Time as Vaporware** award. The two-chip set appears to offer about the same performance as SuperSPARC at a slightly lower price, but Ross will sell the chips only as part of MBus processor modules, making comparison with processor chips difficult. Sun continues to reject hyperSPARC for its own systems, leaving Ross to pursue only low-volume opportunities.

Recognizing the lack of high-volume SPARC vendors other than itself, Sun is attempting to increase the adoption of SPARC. The company is now offering one-stop shopping for all SPARC processors and support chips used in its own systems, including design kits and (gasp!) early access to future designs. Addressing the software side, Sun says that Windows NT will be available on SPARC by 1995. Unfortunately, all current SPARC chips are big-endian and thus unsuited for NT; the company indicates that UltraSPARC will be the first bi-endian SPARC processor.

Although Sun is trying to improve the outlook for SPARC, its strategy seems confused. Its low-cost systems could be competitive with PCs, but they run the Solaris operating system and use SBus for expansion. Sun rightly reckons that Windows NT is a high-end OS, linking its NT strategy to the costly UltraSPARC, but by the time that chip is ready, NT will be headed for the mainstream. Selling its chip sets is a good idea, but its current offerings are best suited for cloning Sun workstations, not a market that needs to be expanded.

Perhaps 1994 will provide further insight. Sun is said to be considering adding a bi-endian switch to the SuperSPARC-2, a 65-MHz, 120-SPECint92 processor due to hit the streets in 3Q94. A new microSPARC-2, with a bi-endian switch and a PCI interface instead of SBus, could make a nice NT box, but this insight may not occur to Sun until 1995, if ever.

Back to the Future

For most of 1993, HP deserved the **Silent Running** award, as it stood by while the 21064, R4400, and Power2 surpassed the PA-7100 in performance. A few days before Christmas, just in the Nick of time, the reticent company finally revealed its plans to get back into the race *(see **0717MSB.PDF**)*. The newly announced PA-7150, expected to ship this spring, could even return HP to the performance lead that it held as recently as 12 months ago.

The 125-MHz 7150 is projected to exceed 135 SPECint92, earning it the **Chuck Yeager** award as the first scalar processor to break the 1.0 SPECint/MHz barrier. (Like the 7100, the 7150 can dispatch two instructions

Processor	IBM Power2	MIPS TFP	MIPS R4400	HP PA-7150	Digital 21064A	Super SPARC+	hyper SPARC	Intel Pentium
Pipeline Frequency (max)	71.5 MHz	75 MHz	150 MHz	125 MHz	275 MHz	60 MHz	66 MHz	66 MHz
Number of Pipe Stages	5 stages	5 stages	8 stages	5 stages	7 stages	4 stages	6 stages	5 stages
Max Instructions per Cycle	6 issue	4 issue	1 issue	2 issue	2 issue	3 issue	2 issue	2 issue
Max Load/Stores per Cycle	2 mem	2 mem	1 mem	1 mem	1 mem	1 mem	1 mem	2 mem
Max Integer Math per Cycle	2 int	2 int	1 int	1 int	1 int	1 int	1 int	2 int
Max FP Math per Cycle	2 FP	2 FP	1 FP	1 FP	1 FP	1 FP	1 FP	1 FP
On-Chip I-Cache	32K	16K	16K	none	16K	20K	8K	8K
On-Chip D-Cache	none	16K	16K	none	16K	16K	none	8K
Peak On-Chip Cache B/W	2,288 MB/s	2,400 MB/s	2,400 MB/s	n/a	4,400 MB/s	1,440 MB/s	533 MB/s	2,667 MB/s
Peak Off-Chip Cache B/W	2,288 MB/s	1,200 MB/s	1,200 MB/s	2,000 MB/s	1,100 MB/s	480 MB/s	533 MB/s	533 MB/s
Branch Cache Entries	none	1024 × 1	none	none	4096 × 2	none	none	256 × 2
Total TLB Entries	640 entries	384 entries	48 entries	136 entries	48 entries	64 entries	64 entries	96 entries
IC Process Type	CMOS	CMOS	CMOS	CMOS	CMOS	BiCMOS	CMOS	BiCMOS
Feature Size (drawn)	0.60 μm	0.70 μm	0.60 μm	0.80 μm	0.50 μm	0.72 μm	0.65 μm	0.80 μm
Number of Metal Layers	5 metal	3 metal	3 metal	3 metal	4 metal	3 metal	2 metal	3 metal
Transistor Count	5,571,000(1)	3,430,000(2)	2,300,000	850,000	2,800,000	3,100,000	1,700,000(2)	3,100,000
Die Area	483 mm²(1)	596 mm²(2)	184 mm²	196 mm²	164 mm²	256 mm²	327 mm²(2)	294 mm²
Estimated Mfg Cost	$470(1)	$1,010(2)	$140	$150	$160	$275	$160(2)	$430
Package	736 pin MCM	2 × 591 pin PGA	447 pin PGA	504 pin PGA	431 pin PGA	293 pin PGA	208, 312 TAB	279 pin PGA
SPECint92	126 int	>90 int	96 int	>135 int	~170 int	77 int	65 int	67 int
SPECfp92	260 fp	>200 fp	105 fp	>200 fp	~290 fp	98 fp	86 fp	62 fp
1K List Price	n/a	n/a	$860(4)	n/a	$1586	$999	$1,595(5)	$898
Vendor	IBM(3)	Toshiba	Toshiba(4)	HP(3)	Digital	TI, Sun	Fujitsu	Intel
Volume Shipments	4Q93	1Q94	3Q93	2Q94	3Q94	4Q93	3Q93	2Q93

Table 2. A list of key parameters for current and announced high-end RISC processors and Pentium. (1) Includes three processor chips but not the custom cache-memory chips. (2) Includes two chips. (3) IBM and HP do not intend to market these chips but may sell them to partners. (4) Toshiba price; IDT and NEC pricing is slightly higher. (5) Price of complete MBus module with 256K of cache. (Source: vendors)

per cycle only on floating-point code.) This doesn't mean that the CPU is executing more than one instruction per cycle; it indicates that the 71x0 CPU and memory system are more efficient, on a per-cycle basis, than the CISC-based VAX 780 that is used as the unity value for the SPEC suite. And you thought RISC instructions are less powerful than CISC instructions!

At the low end of the scale, HP announced sampling of its PA-7100LC chip, which it first revealed 14 months earlier. As with its other chips, HP will provide the 7100LC only to its partners, members of the Precision RISC Organization (PRO). Dual integer units help propel the 7100LC to its relatively lofty performance, which is in tight competition with the PowerPC 601 as the **Fastest Low-End Processor** in Table 3.

Hitachi revealed two new processors, the first PA-RISC chips designed outside of HP. The high-end HARP-1 has dual integer units but delivers about the same performance as the year-old PA-7100 design and is much more expensive to build, earning the **Too Little, Too Late** award.

The PA/50L shows more promise with a lower-cost design, but the first parts, which run at 33 MHz, appear to have performance similar to a 486's. (Hitachi has not released measured SPEC ratings for either chip.) The company is planning to boost the PA/50 to 60 MHz by switching to a 5-V design, which could create an attractive price/performance point for low-end systems. Hitachi has not yet announced price or availability for either of these processors.

HP seems to have hit a dry patch in the past year; neither a new core CPU nor a new 0.6-micron CMOS process were available in time to provide a performance boost to the PA-7100. Some impressive compiler work may save the day, however, and the 7150 and 7200 show promise for the coming year. These chips should help HP maintain its share in the workstation and server markets.

Like Sun, HP lacks a strategy for reaching the high-volume desktop market, having no support for PC buses or operating systems. The company is investigating technologies such as PCI and Windows NT, and has even committed to making the 7100LC and future chips bi-endian, but it refuses to commit to delivering these PC technologies. HP is also the only company trying to support a major RISC architecture without marketing its chips openly, making it the company **Most Likely to Get a Hernia** while carrying its architecture.

Night of the Living Dead

Motorola finally began shipping the 88110 last January, 27 months after first revealing the part, clearly winning the hotly contested **Longest Time as Vaporware** award. Initial shipments were made at 40 MHz, and the chip has only recently begun shipping at its target frequency of 50 MHz. Perhaps we should simply retire this award in honor of Motorola's performance.

Last year, the 88110 nearly won the award for Most Likely Casualty and was saved from oblivion only by

Processor	MIPS R4200	MIPS R4600	PowerPC 603	PowerPC 601	HP PA-7100LC	SPARC MS-2	DECchip 21066	Intel Pentium
Pipeline Frequency (max)	80 MHz	100 MHz	80 MHz	80 MHz	80 MHz	85 MHz	166 MHz	66 MHz
Number of Pipe Stages	5 stages	5 stages	5 stages	5 stages	5 stages	5 stages	7 stages	5 stages
Max Instructions per cycle	1 issue	1 issue	3 issue	3 issue	2 issue	1 issue	2 issue	2 issue
Max Load/Stores per cycle	1 mem	1 mem	1 mem	1 mem	1+ mem(2)	1 mem	1 mem	2 mem
Max Integer Math per cycle	1 int	1 int	1 int	1 int	2 int	1 int	1 int	2 int
Max FP Math per cycle	1 FP	1 FP	1 FP	1 FP	1 FP	1 FP	1 FP	1 FP
On-Chip I-Cache	16K	16K	8K	32K	1K	16K	8K	8K
On-Chip D-Cache	8K	16K	8K	unified	none	8K	8K	8K
Peak On-Chip Cache B/W	1,280 MB/s	1,600 MB/s	1,280 MB/s	2,560 MB/s	640 MB/s	1,360 MB/s	2,666 MB/s	2,667 MB/s
Peak Off-Chip Cache B/W	320 MB/s	400 MB/s	640 MB/s	640 MB/s	640 MB/s	n/a	333 MB/s	533 MB/s
Integrated System Logic	none	none	none	none	cache cntl, memory	memory, SBus	cache cntl, mem, PCI	none
IC Process Type	CMOS	CMOS	CMOS	CMOS	CMOS	CMOS	CMOS	BiCMOS
Feature Size (drawn)	0.60 µm	0.64 µm	0.50 µm	0.60 µm	0.80 µm	0.50 µm	0.68 µm	0.80 µm
Number of Metal Layers	3 metal	3 metal	4 metal	5 metal	3 metal	3 metal	3 metal	3 metal
Transistor Count	1,300,000	1,850,000	1,600,000	2,800,000	800,000	2,300,000	1,747,000	3,100,000
Die Area	78 mm^2	77 mm^2	85 mm^2	121 mm^2	196 mm^2	233 mm^2	209 mm^2	294 mm^2
Estimated Mfg Cost	$40	$43	$55	$100	$140	$195	$210	$430
Package	208 pin PQFP	208 pin MQUAD	240 pin CQFP	304 pin CQFP	432 pin PGA	321 pin PGA	287 pin PGA	279 pin PGA
SPECint92	~55 int	>68 int	~75 int	~85 int	~84 int	~61 int	~70 int	67 int
SPECfp92	~30 fp	>60 fp	~85 fp	~105 fp	~130 fp	~53 fp	~105 fp	62 fp
List Price (1,000 units)	$80	$240 (10K)	n/a	$600 (est)(1)	n/a	n/a	$424	$898
Vendor	NEC	IDT, Toshiba	Moto, IBM	IBM, Moto	HP(3)	Fujitsu, Sun	Digital	Intel
Volume Shipments	2Q94	1Q94	3Q94	1Q94(1)	1Q94	1Q94	1Q94	2Q93

Table 3. Many RISC vendors announced chips expected to be used in low-cost desktop systems, competing directly with high-end PCs. The table includes Pentium, the leading CISC chip, for reference. (1) 66-MHz version shipped 4Q93 for $450. (2) Can issue two memory operations only if they access the same doubleword. (3) HP does not intend to sell its chips on the merchant market. (Source: vendors)

Data General. Motorola's most faithful customer decided to stick with the 88000 architecture to protect its installed base, a whopping 20,000 Aviion systems. Still, the architecture appears to have little future, even at DG; we give it the **George Romero** zombie award.

The winner of last year's Most Likely Casualty award was Intel's i860. After 12 months with a flat brain scan, the i860 is officially declared dead, earning the **What Would You Like on Your Tombstone?** award.

Star Trek: The Next Generation

The stars are aligning to deliver a fleet of high-end processor announcements around the end of 1994. The major RISC vendors are all aiming for a common goal: a four- to six-issue superscalar processor with branch prediction and speculative execution to keep the pipeline full. All expect to exceed 200 SPECint92 and hope to deliver samples by the end of the year. These projects include Digital's 21164 (EV-5), MTI's T5, Sun's UltraSPARC, and the PowerPC 620. Interestingly, Intel's P6 is on a similar schedule, although its CISC handicaps are expected to keep it down around 150 SPECint92.

Can the RISC vendors pull it off? None has yet taped out, so it's hard to say. Given the number of enterprises aiming for this performance point, it seems likely that some will succeed. Given past history, however, it is certain that some will be late and have problems reaching their clock frequency and performance targets. We can also guess that all these processors will be quite expensive, probably selling for around $1,000 to start. While it is important for RISC vendors to demonstrate a higher high end than Intel's, these pricey chips will be confined to workstations and servers, at least initially.

The volume price points will be filled by chips like the R4600, which shows that a clean, simple design can deliver respectable performance at a much lower cost than these macho superchips. The challenge for RISC vendors in 1994 is to improve the availability of software applications for their architectures; until then, any hopes for high volumes will be dashed by the overwhelming software advantage of the x86. ♦

Major RISC Events of 1993

Sun details extensive roadmap for SPARC processors *(see **070404.PDF**)* and plans to sell processors on the open market *(see **071501.PDF**)*.

SuperSPARC hits 60 MHz, TI cuts prices *(see **0709MSB.PDF**)*; Sun announces microSPARC-2 *(see **071501.PDF**)*; Weitek delivers upgrade chip for SPARCstation 2 and IPX systems *(see **070902.PDF**)*.

SPARC Version 9 revealed, with 64-bit extensions and new instructions *(see **070201.PDF**)*; Intergraph to port Windows NT to SPARC *(see **0710MSB.PDF**)*.

Cypress sells Ross Technology to Fujitsu *(see **0707MSB.PDF**)*; Ross ships hyperSPARC processor modules *(see **071502.PDF**)*.

Andy Heller leaves HaL Computer under cloud *(see **0710MSB.PDF**)*; Fujitsu absorbs HaL *(see **0715MSB.PDF**)*.

SGI reveals TFP for high-performance floating-point *(see **070202.PDF** and **071102.PDF**)*.

MIPS Technologies opens NT design center *(see **0703MSB.PDF**)*; Acer, Toshiba, and Deskstation deploy system-logic chip sets for MIPS processors *(see **070501.PDF**, **0709MSB.PDF**, and **0714MSB.PDF**)*.

MIPS Technologies announces low-cost R4200 processor *(see **070701.PDF**)*; IDT, Toshiba announce Orion as the R4600 *(see **0714MSB.PDF**)*.

Motorola, IBM sample PowerPC 601 *(see **070602.PDF**)* and unveil PowerPC 603 *(see **071402.PDF**)*; IBM announces first PowerPC systems *(see **0713MSB.PDF**)*.

PowerPC gains support for Windows NT and PCI *(see **071601.PDF**)*; Prep document specifies compatible PowerPC systems *(see **071704.PDF**)*.

IBM boosts high-end performance with its multichip Power2 processor *(see **071301.PDF**)*.

Digital reveals PCI chip sets for its Alpha processors *(see **070904.PDF**)*, announces the 21066 CPU with integrated PCI *(see **071201.PDF**)*; Digital announces 275-MHz 21064A will reach 170 SPECint92 *(see **0714MSB.PDF**)*; Mitsubishi to second-source Alpha processors *(see **0704MSB.PDF**)*.

HP reveals high-speed PA-7150 CPU, announces low-cost PA-7100LC, discloses PA-RISC roadmap *(see **0717MSB.PDF**)*; Hitachi previews its first PA-RISC chip, the high-end HARP-1 processor *(see **071104.PDF**)*.

Motorola finally announces 88110 *(see **0702MSB.PDF**)* and Data General uses it *(see **0709MSB.PDF**)*.

