Intel Reveals Successor to 960KA

J Series More Than Doubles Performance at Same Price Points

by Michael Slater

Intel has boosted the midrange of its successful 960 embedded processor family by creating a single-issue version of its superscalar 960CA and mating it to the bus interface of the low-end 960KA. The new family, dubbed the J series, more than doubles the performance of the KA at the same clock rate, and it also offers higher clock speeds and clock-doubled operation up to 50 MHz.

The J-series chips, code-named P100 and also called Cobra, are priced competitively with the 960KA and will obsolete that part for new designs. None of the new chips has a floating-point unit, so the 960KB will retain its niche, and the 960SA/SB family will continue to hold the low end. The 960CA and CF serve the high end, although the fastest J-series chips will encroach on that territory. The 960CA will remain of interest for new designs primarily because it is pin-compatible with the top-of-the-line CF and future high-end devices.

Table 1 summarizes the 960 family. The J series includes all the features of the superscalar CA core (but not the DMA controller) in a lower-cost, scalar (single-issue) design. As usual with embedded processors, a family of devices has been created from a single silicon design. The 960JF is the midrange member of the J series. The JA is a lower-cost version with half as much instruction and data cache, and the JD is the high-end member with an on-chip clock doubler.

The JA is offered only in a 3.3-V version, while the JD requires 5 V; the JF is available for either supply voltage. External clock speed is limited to 25 MHz at 3.3 V or 33 MHz at 5 V. With the clock-doubled version, the CPU core can run at up to 50 MHz.

According to Intel's benchmarks, the 25-MHz JF delivers 2.6 times the performance of a 960KA at the same clock speed using 120-ns ROM, or 2.2 times the 960KA using 80-ns DRAM (based on simulations of Postscript "golfer" page rasterization). The clock-doubled 960JD, running at 50 MHz internally but with the same 25-MHz bus and memory system, delivers over three times the performance of the 960KA. A networking protocol benchmark shows similar performance gains.

Cost-Reducing the CA Core

The 960 K-series processors were an outgrowth of Intel's ill-fated BiiN venture to build fault-tolerant computers (see MPR 4/88, p. 1), and they contain several features, such as a specialized MMU, that were not documented for the embedded market. The later S series cost-reduced the K series by eliminating unused features and moving to a 16-bit data bus (see MPR 10/17/90, p. 15). The current high end of the line, the C series, is a second-generation implementation that provides superscalar execution in addition to a faster pipeline design (see MPR 8/89, p. 1). The CF was the first 960 to include a data cache and to use a 0.8-micron process.

	80960SA/SB	80960KA/KB	80960CA	80960CF	80L960JA	80960JF	80L960JF	80960JD
CPU Core	Cost-reduced K-series core	First Generation	Superscalar	Superscalar	CA-Derived Scalar	CA-Derived Scalar	CA-Derived Scalar	CA-Derived Scalar
FPU	SB only	KB Only	no	no	no	no	no	no
Instr. Cache	512 Byte DM	512 Byte DM	1K 2-way	4K 2-way	2K 2-way	4K 2-way	4K 2-way	4K 2-way
Data Cache	none	none	none	1K	1K	2K	2K	2K
Data RAM	none	none	1K	1K	1K	1K	1K	1K
Register Sets	4	4	5–15	5–15	8	8	8	8
DMA	no	no	4 Channels	4 Channels	no	no	no	no
Buses	32/16 adrs/data mux	32/32 adrs/data mux	32 adrs, 32 data	32 adrs, 32 data	32/32 adrs/data mux	32/32 adrs/data mux	32/32 adrs/data mux	32/32 adrs/data mux
Clock (MHz)	10, 16, 20	16, 20, 25	16, 25, 33	16, 25, 33, 40	16, 25, 33	16, 25, 33, 40	16, 25, 33	33, 40, 50
Clock Doubler	no	no	no	no	no	no	no	yes
VAX MIPS*	7 (16 MHz)	12 (25 MHz)	37 (33 MHz)	60 (40 MHz)	28 (33 MHz)	33 (40 MHz)	28 (33 MHz)	41 (50 MHz)
Supply Voltage	5V	5V	5V	5V	3.3V	5V	3.3V	5V
Typ. Power	1.1W (20MHz)	1.8W (25MHz)	3.8W (33MHz)	5.0W (40MHz)	0.5W (33MHz)	1.2W (33MHz)	0.5W (33MHz)	1.9W (50MHz)
Price (10,000)	$9.75/$11.70/ $12.80 (SA) $14.45/$15.90 (SB-10,16)	$18.55/$20.40/ $22.45 (KA) $20.40/$22.45/ $24.70 (KB)	$43.90/ $57.10/ $84.60	$52.70/ $87.90/ $125.40/ $175.80	$16.60/ $20.80/ $25.95	$24.90/ $31.10/ $38.95/ $48.65	$27.40/ $34.25/ $42.90	$29.45 (PQFP) $44.45 (PGA)/ $50.30 (PGA)/ $57.35 (PGA)
Availability	Now	Now	Now	Now	3/95 (6/95–33MHz)	12/94 (6/95–40MHz)	3/95 (6/95–33MHz)	6/95

Table 1. The four members of the J series, at right, offer many of the CA's features in a package and price to match the KA. *VAX MIPS based on Dhrystone 2.1 in a system with zero-wait-state SRAM.

 © 1994 MicroDesign Resources

	960SA/SB	960KA/KB	960CA	960CF	960Jx
Transistors	346,000	350,000	600,000	800,000	750,000
Die Size	51 mm^2	59 mm^2	137 mm^2	120 mm^2	64 mm^2
Process	1.0-µm, 2 metal	1.0-µm, 2 metal	1.0-µm, 2 metal	0.8-µm, 3 metal	0.8-µm, 3 metal
Package	80-pin PQFP or 84-pin PLCC	132-pin PGA or PQFP	168-pin PGA or 196-pin PQFP	168-pin PGA or 196-pin PQFP	132-pin PGA or PQFP

Table 2. The more advanced process allows the Jx to pack many more transistors on a die only slightly larger than the Kx and half the size of the CA.

The J-series designers started with the C-series CPU core and stripped it down to a single-pipeline, single-issue design. At the same time, a few other changes were made to reduce cost and power consumption, and a few new features were added to boost performance.

Because the J-series chips are built in a 0.8-micron process technology, they are able to deliver much more performance than the K series with a slightly larger die size, as Table 2 shows. The 960JD will outperform the CA in some applications and approach the performance of the CF, broadening the range of applications that will be able to use the lower-cost J-series chips. With much of Intel's 486 and Pentium production shifting to new 0.6-micron fabs, the 0.8-micron lines have fully depreciated capacity available for the 960 line.

The small die size is achieved without a full-custom, hand-packed layout: to reduce time-to-market and enable easy customization, the entire design is implemented with compiled VHDL. Customers that purchase more than 500,000 units per year (i.e., Hewlett-Packard and very few others) will be able to add their own custom logic to the design. This strategy will enable Intel to compete, for the first time, with custom integration programs such as Motorola's FlexCore and LSI's CoreWare, though only for the highest-volume applications.

Figure 1 shows the block diagram of the 960Jx. The pipeline design and fast multiply/divide unit are borrowed directly from the CA, but the register and memory configuration is different. The CA uses on-chip data RAM to store additional register sets in addition to acting as a general-purpose data memory, and a wide, 128-bit bus allows quick transfers between the cache and the register file. In the J series, dedicated memory is provided for eight register sets. There is a short 128-bit-wide bus between the register file and the local register cache, but the buses from the caches and SRAM to the CPU core are only 32 bits wide.

Optimizing Instruction Execution Speed

Although the J series does not issue multiple instructions simultaneously, the multiply/divide unit can run concurrently with the main execution unit. This allows other instructions to execute in parallel with long-latency operations. Like all 960 processors, but unlike most others, register scoreboarding allows the CPU to continue execution while a load instruction is waiting for a memory access to complete if the instructions following the load do not use the loaded data.

The J series has a three-port register file; because it is a single-issue machine, the six-port file of the C series

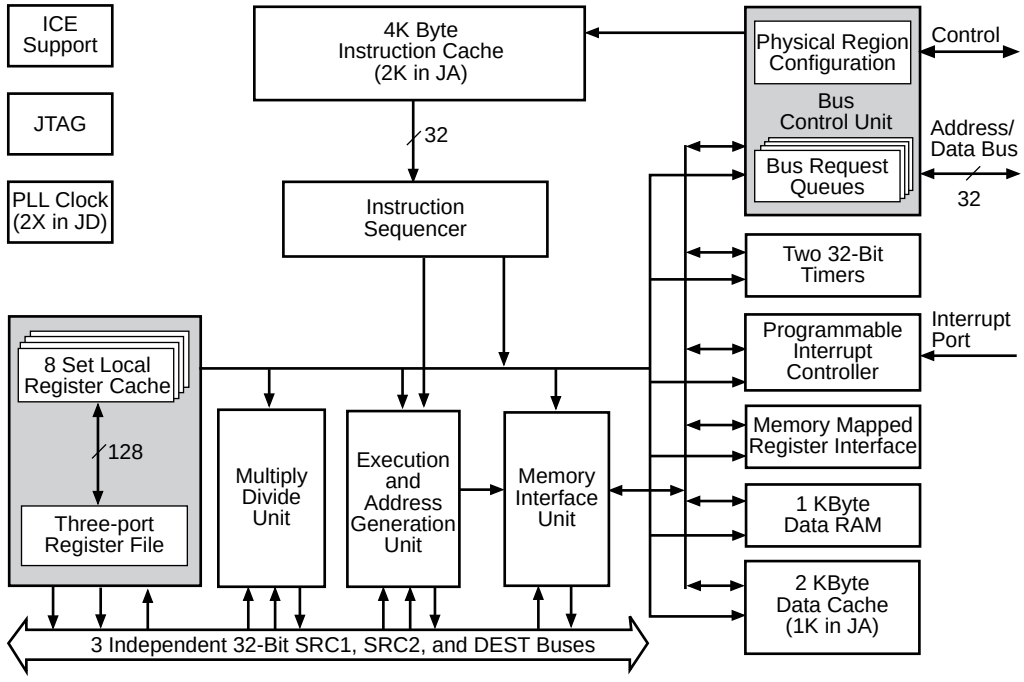

Figure 1. The 960Jx combines a scalar version of the 960CA core with a 960K-series bus interface and peripheral set.

 © 1994 MicroDesign Resources

is not needed. The three-port file enables some instructions to execute more quickly than on the K series, which has only a two-port file. The J series implements more complete register bypassing, cutting another clock cycle off of some instructions. Address calculations are also performed more quickly on the J series; in fact, it is even faster than the C series for some addressing forms.

Table 3 summarizes the instruction performance of the three 960-family CPU cores. The J series matches the C series performance on all ALU operations, although the C series retains an advantage in being able to execute three instructions per clock cycle (given a propitious mix of one branch, one ALU operation, and one load/store instruction). Branch, call, and return instructions are faster than the K series but not as fast as the C series; the C-series superscalar core allows some branch execution to be completely hidden, and calls and returns that include a register-file swap are significantly faster on the C series.

The J series also matches the C-series performance on the more RISC-like BAL (branch and link) instruction, and is even faster on the BX instruction, used for a RISC-style return (without restoring a register set). Load instructions match or exceed the C-series performance.

The J-series instruction and data caches are similar to those in the C series. The 4K instruction cache is two-way set-associative and allows either set to be locked, so critical code can be kept in the cache while the other set operates as a direct-mapped cache. The 2K data cache is direct mapped and uses a write-through, write-allocate policy. A separate valid bit is provided for each word, and only the requested data is filled, not the entire line. (Bytes and 16-bit half-words are promoted to words, but words are not promoted to cache lines.)

Like the C-series processors, the Jx chips have no MMU. A bus width of 8, 16, or 32 bits is set independently for each of eight fixed 512K regions (the CA provides 16 regions). In addition, the J-series chips provide control of two logical memory regions, whose base addresses can be set with 4K granularity. The default byte ordering of the processor is set to big- or little-endian via a configuration register; for each logical memory region, the byte ordering for data accesses can optionally be set to the opposite of the default. Logical memory regions also control cachability. Like all 960 processors, the Jx chips support unaligned loads and stores.

Instruction Set Extensions

Intel has developed its own compilers for the 960 family, and the designers of the J series worked with the compiler designers to evaluate potential additions to the instruction set. They settled on a few additions that were usable by the compiler and yielded significant performance improvements on networking or imaging applications. The new instructions are:

	K Series	J Series	C Series
Most register ops	1–2	1	1
shift, setbit, clrbit	2–3	1	1
multiply (16×32/32×32)	9–21	2/4	2/4
scanbit	8–14	1	1
branch & link/bx(base)	2–8	2	2/4
call	9	7	4
return	7	5	4
branch	2	2	0–2
branch taken	3	2	0–2
branch not taken	2	1	0–2
branch miss latency	6	3	3
ld (reg)	5	1/2	2
ld disp (32-bit offset)	5	2/3	2
ld disp + (reg)	6	2/3	3
ld disp + (reg)*scale	6	2/3	3

Table 3. The J series offers instruction execution speeds (in clock cycles) comparable to the C series on most instructions. For loads, the two values are for data not needed/needed by next instruction.

- Compares for bytes or 16-bit words. (Previous chips have 32-bit compare only.)
- Conditional add and subtract (signed and unsigned).
- Conditional select, which loads the destination register from one of two source registers, as determined by the condition.
- Byte swap, which reverses the order of the four bytes within a word to convert between little- and big-endian data formats.
- Halt, which puts the CPU in a low-power state (with power consumption reduced by over 90%) until it is awakened by an interrupt or reset.

The new compare instructions eliminate the need to mask unused bits when comparing quantities smaller than a full word. The conditional instructions eliminate conditional branches in common situations, which keeps the pipeline flowing and thereby improves performance as well as code density. These instructions can also implement conditional moves. Byte swap is especially useful in networking applications that have to work with data using different byte ordering. Intel estimates that the new instructions provide a 15–20% performance boost in many applications.

Extending the C Series Bus and Peripherals

The Jx chips provide eight interrupt inputs plus a nonmaskable interrupt. As in other 960 processors, the interrupt inputs can each vector to a dedicated address, or an expanded mode allows a vector to be supplied. The K-series chips implement expanded-mode vectoring, with an 8259A interrupt controller providing the vector on the data bus; the J-series devices follow the scheme used in the C series, with the vector provided on the interrupt pins. A mixed mode can also be selected, in which three pins have dedicated vectors and the other five operate in expanded mode. Interrupt latency is less than 1 µs, including prioritization and saving of processor state.

 © 1994 MicroDesign Resources

A new feature in the J series is the addition of two 32-bit timers, which can be programmed as single-shot or auto-reload timers and can generate an interrupt when the terminal count is reached. The bus clock can be prescaled by 1, 2, 4, or 8 to provide the timer clock.

The J-series processors are bus-compatible, but not pin-compatible, with the K-series chips, so they can't be dropped into existing sockets, but existing designs can be easily modified. Additional signals have been added to give logic analyzers more information about program flow. The function of the READY signal has been extended to allow wait states to be added after the last cycle of a transfer, giving slow devices more time to get off the bus. This eliminates the need for external buffers in systems with devices, such as mask-programmed ROMs, that can't get off the bus quickly enough to let the processor output an address in the next cycle after a read.

Another new signal is BSTAT (bus status), which indicates that the processor is about to stall due to unavailability of the system bus. This signal enables the bus arbiter in a system with multiple masters to optimize the use of the bus bandwidth in its granting of bus ownership to a particular processor.

The clocking also has been improved. The clock input runs at the bus clock, rather than twice that rate as in the K series, and bus timing is specified relative to the input clock. This change simplifies system design compared with previous chips that generated a clock output to which bus timing was referenced.

Cementing the 960's Lead

Intel's 960 family has a commanding lead in the embedded RISC market, with 1993 shipments of 4.6 million units (according to Dataquest) accounting for twice as many chips as all other embedded RISC processors combined. A significant part of this lead is due to a single design win, HP's LaserJet 4, which is the highest-volume RISC application yet. The 960 family is also widely used in networking and communication products, PC I/O devices such as RAID disk controllers, and some of Sega's arcade (not home) video games.

Because each company uses different benchmarks and system configurations, it is difficult to make exact performance comparisons between AMD's 29000 and Intel's 960 processors. Also, the Jx chips won't ship in volume for many months, and AMD could have new versions by then.

Both companies provide MIPS ratings based on Dhrystone 2.1, but Intel uses systems with zero-wait-state SRAM while AMD uses more realistic DRAM memory systems. For the Jx devices, Intel claims that Dhrystone performance is just as good with a slower memory system, since the program fits in the cache. At best, Dhrystone is a poor benchmark, but there are no other benchmarks widely used by embedded CPU vendors for cross-architecture comparisons.

Price & Availability

Samples of the 960JA and JF are promised for September except for the highest clock rates (33 MHz at 3.3 V, 40 MHz at 5 V), which are planned for December; JD samples also are due in December. See Table 1 for pricing and production availability.

For more information, contact your local Intel sales office or call 800.628.8686. Information can also be obtained from Intel's FAXBack service at 800.628.2283; request document number 2068.

For each architecture, there is a range of implementations that covers a similar performance spectrum. AMD's new 29040 appears to be significantly faster than even the high-end JD, but it is also much more expensive; the J series seems best matched against the 29030.

The J series strengthens the 960's position by more than doubling the performance of the K-series chips at a comparable cost. The larger caches enable this performance boost without more expensive memory systems. The one hole that remains in the product line is a chip with high-performance floating point, but relatively few embedded applications demand this feature.

Intel's next step will be to extend the high end of the family with a more aggressive superscalar design, codenamed the P110, which will be unveiled at the Microprocessor Forum this fall. One member of the P110 family will include a high-performance FPU, filling that gap. Having a higher-performance CPU in the family will become more important as PowerPC makes its move into the embedded arena, AMD delivers its superscalar 29000 implementation, and embedded MIPS processors advance from the R3000 core to the R4000.

Intel has been slow in integrating on-chip peripherals, and this oversight may provide its competitors with one avenue of attack. Motorola's 68300 family is the champion in functional integration; AMD's 29200 family and LSI Logic's LR33000 family also have gone far beyond Intel's 960 in this regard. Intel says that most of its customers build an ASIC to work with the processor, and that these customers want Intel to focus on providing the most performance for the lowest cost. Intel is taking a tentative step toward functional integration, though, in offering to add custom logic to the J-series processors for high-volume users. High-integration products based on the Jx core will be introduced later this year.

The high-performance embedded processor market is becoming increasingly crowded, but Intel is well positioned to retain its lead by offering a broad range of price/performance points and excellent development support. The J series is one sign of how Intel's volume lead allows it to invest heavily in developing new cores, which should further cement its position. ♦

 © 1994 MicroDesign Resources