Most Significant Bits

200-MHz R4400 to Ship This Fall

MIPS Technologies (MTI) announced that IDT, Toshiba, and NEC have begun sampling the 200-MHz R4400 that was demonstrated at Comdex last fall *(see **0716MSB.PDF**)*. The new speed grade was originally expected to be in production by midyear, but yields have been poor in the 0.4-micron process used for the 150-MHz part, forcing a move to a new 0.35-micron process that has delayed the schedule. Preliminary measured benchmark ratings are 117 SPECint92 and 131 SPECfp92. According to a suite of Windows NT benchmarks run by MTI, the R4400/200 outperformed a 90-MHz Pentium system by a factor of 1.3–3.1, depending on the application.

The thinner oxides of the new process require the new chip to run only at 3.3 V, although the 150-MHz version (using a 0.6-micron process) is available in a 5-V version. Power dissipation at 200 MHz is just 8 W. Although the standard version of the R4400 is pad-limited, Toshiba has managed to shrink its new part by 22%, to 134 mm^2, by interleaving the pads around edge of the die. NEC and IDT plan to produce the larger version with a standard pad ring. According to the MPR Cost Model *(see **071004.PDF**)*, this version costs around $150 to build, about the same as the 150-MHz chip; Toshiba's smaller die reduces costs by about 12%. These costs assume reasonable yields at that clock rate.

The fast R4400 is a bridge until the next-generation T5 is available. Contrary to previous reports, T5 has not taped out and is not expected to ship before mid-'95. The R4400 may be essentially obsoleted even sooner when IDT and Toshiba raise the clock frequency of their R4600 by shrinking it to a 0.5-micron process; a 175-MHz version should match the integer performance of the 200-MHz R4400 at a lower cost, leaving the more expensive part for only high-end workstations and MP servers.

The performance of the new R4400 falls well behind that of the PowerPC 604, Digital's 21064A, and HP's PA-7200, all of which are due at about the same time and should deliver 160 SPECint92 or more. Toshiba, the only MIPS vendor willing to quote pricing for the 200-MHz R4400SC, says that it initially will cost $1,950 in quantities of 1,000, nearly three times the price of a comparable 150-MHz part or a 200-MHz 21064 from Digital. Production is planned for the third quarter but, as with the 150-MHz R4400, there may be a long ramp; the ridiculously high prices will keep anyone from buying in volume until the prices drop, hopefully quickly.

NEC also acknowledged that volume shipments of its own R4200 have been delayed until 3Q94 to work out bugs that affect Windows NT, although the current version reportedly works fine for most embedded applications. The R4200 falls quite short of the R4600 in performance, and NEC has yet to announce plans to increase its clock rate. NEC is clearly hampered by lack of access to the R4600, which was designed by start-up QED with funding from IDT and Toshiba, and may need to pick up that design at some point.

R8000 Sets SPECfp92 Record

MTI also announced availability of the R8000 processor, previously known as TFP *(see **071102.PDF**)*. This two-chip processor, intended for high-end scientific applications, was originally expected to ship by the end of last year but is just now reaching production. The performance of the R8000 is much better than expected, however. In fact, the chip set achieves 311 SPECfp92, exceeding the previous record of 260 set by IBM's Power2 chip set. On the integer side, the R8000 turns in a more modest 108 SPECint92, just below the R4400/200.

According to MTI, the 75-MHz R8000 offers performance similar to a Cray Y-MP processor on many supercomputer benchmarks, yet systems using the R8000 may sell for as little as one-tenth the price of comparable Cray systems. The chip set achieves this performance through dual FPUs with multiply-add capability, resulting in 300 peak MFLOPS. The pipelined cache can deliver 1.2 Gbytes/s of data to the FPUs.

Unlike other MIPS processors, the R8000 is not yet available on the open market. Toshiba, which is manufacturing the chip set for Silicon Graphics, says that there are no other customers at this time, but that it is willing to offer the chips if there is interest. Potential customers would pay a steep price compared with other microprocessors: the MPR Cost Model *(see **071004.PDF**)* estimates the cost of the R8000 at just over $1,000, so the list price probably would be $2,000–$3,000. Even at that price, the processor is attractive to minisupercomputer vendors that, along with SGI, will put pressure on Cray's traditional supercomputers.

Apple and IBM Demonstrate 120-MHz 601

At a recent trade show, Apple and IBM showed a Macintosh using a PowerPC 601 running at 120 MHz, but availability of the processor at that clock rate has not been announced. IBM plans to ship 100-MHz 601 processors in the fall, and the frequency distribution typically yields a few chips that could run faster.

It isn't clear that this fast 601 will ever become a product. One issue, of course, is whether IBM can yield the part reliably at 120 MHz; the move from 0.7-micron to 0.5-micron should provide enough headroom to raise the frequency from 80 MHz in the old design. A bigger concern is that, at 120 MHz, the integer performance of the 601 will come close to that of an 80-MHz 604, a part

that will probably be the low speed bin of that design. On floating-point benchmarks, the 120-MHz 601 should be better than the slowest 604s.

Motorola, which has no plans to fabricate its own 601 chips (though it resells IBM's silicon), no doubt would prefer to shift the emphasis to the 604, which both companies will make. IBM, on the other hand, may prefer the 601 for this price point, since its estimated manufacturing cost is less than half that of the 604 *(see **080501.PDF**)*. This may be the first opportunity for the two companies' desktop PowerPC strategies to diverge.

Motorola Reportedly Developing 603+

Motorola is reportedly developing, at Apple's urging, an enhanced version of the 603 with larger caches and a higher clock rate. With 90-MHz Pentium notebooks likely to show up at about the same time as the first PowerPC PowerBooks, today's 603 wouldn't provide leadership performance even for native code.

According to information obtained by *Macweek*, the 603's performance is particularly poor when emulating 68K and x86 programs. These emulators are hard on the caches because their large branch tables can overflow the instruction cache, and the data cache must hold both instructions and data for the emulated program. The small caches in the 603 (8K instruction and 8K data) yield much lower performance during emulation than the 32K unified cache in the 601, even though the 603 has a slightly faster CPU core.

The current 603 is built in a 0.65-micron (drawn) process. (Motorola and IBM often call this a 0.5-micron process, referring to the effective gate length, but by industry-standard terminology it is a 0.65-micron process.) A true 0.5-micron process is planned for the 620, and IBM is using a variant of this process for the 100-MHz 601 *(see **080504.PDF**)*; the enhanced 603 might use this process to boost the clock rate and enable a larger cache without an increase in die size.

Apple has said that it would ship 603-based PowerBooks and low-cost desktop systems in early 1995, but these performance problems may force it to wait for the 603+. The wait may not be long: assuming that Motorola has already started to make these minor changes, the 603+ design could be ready by the end of the year. The problem is that Motorola doesn't plan to have its 0.5-micron process in production until mid-1995. IBM, however, could manufacture the 603+ on its 0.5-micron line in time for Apple's 1Q95 system shipments.

Cyrix, IBM Deliver First Fruit of Partnership

By taking advantage of IBM's 0.7-micron CMOS-4S process, Cyrix is now able to deliver 66-MHz 486DX2 processors in volume and has announced an 80-MHz DX2 for shipment within the next few months. Both of these parts operate at 3.3 V, reducing power consumption compared with Intel's 5-V DX2 parts. Intel's DX2 line is limited to 50 MHz at 3.3 V and 66 MHz at 5 V, although the company does offer clock-tripled DX4 processors at 75 and 100 MHz, both running at the lower voltage. In a separate announcement, IBM Microelectronics said it will resell Cyrix's line of 486DX2 processors under its Blue Lightning brand name.

The new parts use the M7 core *(see **071101.PDF**)*, which uses a write-back cache instead of Intel's write-through version. Because of the faster system bus (33 MHz versus 25 MHz) and the write-back cache, Cyrix's 66-MHz DX2 outperforms the 75-MHz DX4 on many applications, according to Cyrix. At $249 in 1,000-piece lots, the Cyrix part is just over half the price of the 75-MHz DX4. Cyrix will sell the 80-MHz DX2 for $294, giving it a similar advantage over the 100-MHz DX4. IBM's prices are slightly higher: $270 for the 66-MHz part and $320 for the 80-MHz version. With this aggressive pricing, the new parts should compete well against Intel's DX4, particularly for notebooks.

IBM began manufacturing Cyrix's 486 chips in a 0.8-micron process using two metal layers. The new versions are simply a shrink of this original design to a 0.7-micron process. The companies still plan to develop a new design with three metal layers that should further reduce die size and boost clock speeds to 100 MHz in the same 0.7-micron process *(see **080602.PDF**)*. They expect to ship this version by the end of the year.

NexGen, IBM Finally Come to Terms

Taking the first step in establishing itself as a credible x86 vendor, NexGen has announced that IBM will fabricate its Nx586 and Nx587 chips. NexGen's fab situation has been in limbo for the two months since the company announced its chips, when NexGen's deal with IBM fell through at the last minute *(see **080403.PDF**)*. The companies have now patched things up, securing the startup's access to IBM's world-class 0.65-micron fab line and its Intel patent license. This arrangement gives NexGen the most basic credibility: customers can order parts and expect to receive them.

The next step will be for NexGen to ship enough parts to customers to establish their compatibility with the existing x86 software base. This step will take several months, perhaps longer if compatibility issues arise in the meantime. The company must also show that the 586 meets its performance claims.

On IBM's side, this arrangement appears to be a means to keep its fab lines full. Big Blue has no immediate plans to market the 586 under its own label, as it will do with Cyrix's 486 and M1 chips, but IBM would not rule out such a move in the future. Due to IBM's closer relationship with Cyrix, we believe that Big Blue will not market NexGen's 586 unless the M1 suffers from severe schedule and/or performance problems.

Compaq Ships First Systems with AMD CPUs

The first tangible result of Compaq's agreement to buy microprocessors from AMD has been announced: the Presario 660 and 860 PCs, both based on AMD's 486SX2-66 processor. These are the first systems to use a 66-MHz SX2 chip, and they are likely to remain unique for some time—AMD has granted Compaq a short-term exclusive on these chips, and Intel does not offer them at all.

Given the low margins of the SX chips, AMD probably would have granted this exclusivity whether Compaq wanted it or not. Both Intel and AMD would prefer to use their limited fabrication capacity to build more profitable DX2 chips. When Intel was the only 486SX vendor, it kept its SX chips to low frequencies so system buyers looking for high integer performance would have to buy DX2 systems. But with AMD in the market and looking for ways to convince leading system makers to buy its chips, the SX2 no doubt became a bargaining chip. By getting an exclusive, Compaq gets to make machines at a price/performance point that others can't match.

Digital Eases Alpha Prices

Continuing to reposition its Alpha line to compete on price, Digital has adjusted the prices of its Alpha chips in anticipation of shipments of its new 275-MHz part, which is now priced at $1,192 in 1,000-unit volumes. The 225-MHz speed grade of the 21064A has been replaced by a 233-MHz part, to better match systems with a 66-MHz bus, and now lists for $867.

The new prices are quite aggressive and include a 31% cut for the 200-MHz 21064, which now sells for just $598 but delivers twice the performance of the similarly priced 60-MHz Pentium. The 166-MHz 21064 is now priced at $443, and the 21066, also at 166 MHz, sells for $382. This price leaves the latter chip costing barely more than Intel's 486DX2 yet offering more than twice the performance, plus integrated system logic to boot. These prices must be quite attractive to potential Windows NT system vendors, but the major issue for Digital at this point is building a software base.

Samsung Joins List of ARM Licensees

Korean semiconductor maker Samsung has licensed the ARM processor technology from ARM Ltd. for use in consumer electronics products. The standard ARM processors are currently built by licensees VLSI Technology, GEC Plessey, and Sharp; Cirrus Logic and TI are licensees that will use the ARM core in application-specific chips with additional I/O logic. Samsung plans to use the ARM processor initially in its own peripheral products, including hard-disk drives and laser printers; a PDA is also in the works. Samsung expects to offer its first device with the ARM processor in 1995; chip-level products may follow in 1996.

Samsung is also a PA-RISC licensee but so far has chosen to buy its chips from HP for its own workstation line. Other PA-RISC licensees have developed embedded processors using HP's architecture, but it appears that Samsung will rely on ARM for this product area.

ARM now has a broad range of licensees, covering Europe, Asia, and the United States. Although the two most touted ARM applications—Apple's Newton and 3DO's Multiplayer—have had disappointing sales, ARM is likely to reach critical mass for the long-term success of the architecture through a wide range of embedded applications.

ARM recently scored a potentially important design win when IBM and VLSI Technology entered into an agreement to develop chips for IBM's Serial Storage Architecture (SSA) interface using the ARM core.

Motorola Announces PPC Tools for NT, Mac

To support hardware and software development with PowerPC processors, Motorola has announced a set of development tools for Windows NT and optimizing compilers for Power Macs.

For NT software developers, Motorola is offering a PowerPC C/C++ cross-compiler that runs on x86-based Windows NT systems. The company has promised native versions of the compiler, along with the PowerPC version of Windows NT, in the second half of this year. Motorola's NT compiler combines Microsoft's front end, which ensures syntax-compatibility with Microsoft's x86 compiler, with Motorola's back end, which generates optimized code for PowerPC.

Motorola is offering a similar compiler for Apple's MPW (Macintosh Programmer's Workshop) environment, and a version for MetroWerks' CodeWarrior environment is promised for late this year. Both the NT and Macintosh compilers provide the option to optimize code for a particular PowerPC processor implementation.

Motorola is also providing a device-driver kit for Windows NT, which enables peripheral suppliers to create device drivers to run under the forthcoming PowerPC version of Windows NT, and a Windows NT HAL (hardware abstraction layer) kit, which enables system makers to port the operating system to hardware designs that differ from the PowerPC reference design. The products range in price from $195 to $995 and can be ordered from Motorola at 800.845.MOTO.

Errata: PPC 604, AMD 29240

In our article on the PowerPC 604 *(see **080501.PDF**)*, we erroneously described the IC process used by the chip. The 604 will be built using four metal layers.

In our article on embedded PowerPC chips *(see **080601.PDF**)*, we gave an incorrect performance rating for the 29240. The AMD chip delivers 47.6 Dhrystone MIPS at 33 MHz, making it slightly faster than the embedded PowerPC chips from IBM and Motorola. ♦

