Literature Watch

Buses

Peripheral/channel interfaces take on network roles. Techniques that were conceived as I/O channels are now being drafted into network service. Warren Andrews, *Computer Design,* 6/94, p. 59, 4 pp.

PCI bus offers performance and processor independence—so what's not to like? PCI offers high throughput and good interoperability, but it can be a difficult standard to implement. Jim Kelsey, SystemSoft; *Personal Engineering,* 6/94, p. 73, 4 pp.

Development Tools

Design migration issues influence design-tool selection. Careful selection of software allows porting designs through various tools at various stages. Russ Lindgren, *Personal Engineering,* 6/94, p. 39, 7 pp.

What's an emulator cost? What's it worth? Embedded-systems development becomes costly as processor speeds increase and emulator prices rise dramatically. Jeffrey Child, *Computer Design,* 6/94, p. 105, 8 pp.

Benchtop DSO features full autoranging. A digital and analog oscilloscope automatically varies attenuation and timebase to track changing signals. John Novellino, *Electronic Design,* 5/30/94, p. 131, 2 pp.

Nix physical design flaws before layout. An interconnect-synthesis tool helps build PCBs that function at high clock speeds. Lisa Maliniak, *Electronic Design,* 5/30/94, p. 71, 3 pp.

Object-oriented analysis in the real world. Experience with the Shlaer-Mellor methodology helps designers move from object theory to real-world practice. Michael Lee, Project Technology; *Embedded Systems Programming,* 6/94, p. 24, 8 pp.

DAC focuses on synthesis and ESDA tool advances. This year's Design Automation Conference exposed the trend toward raising the level of abstraction, allowing engineers to ignore implementation details. Lisa Maliniak, *Electronic Design,* 5/30/94, p. 51, 10 pp.

Object-oriented techniques in hardware design. With the advent of HDLs, simulation, and modeling, hardware engineering is in a position to borrow concepts from software programming. Sajaya Kumar, James H. Aylor, et al, University of Virginia; *IEEE Computer,* 6/94, p. 64, 7 pp.

DSPs

DSP-chip directory. Low-cost applications are still dominated by 16-bit DSPs. (Includes directory and specifications of 22 DSP chips.) Jeff Child, *Computer Design,* 5/94, p. 91, 8 pp.

Three DSP RTOSs are ready to merge with Windows. Microsoft and DSP software vendors move toward a standard method for Windows applications to work with different digital signal processors. David Shear, *EDN,* 6/23/94, p. 29, 4 pp.

Memory

Source list: cache RAMs. Modern cache RAMs run at speeds of 20 ns or faster and often incorporate burst counters or even the entire cache controller. (Includes directory of products from 14 manufacturers.) *Electronic Products,* 6/94, p. 36, 6 pp.

Miscellaneous

Real time: further misconceptions (or half-truths). The role of real time in real-time systems easily leads to incompatibilities with non-real-time models. Reino Kurki-Suonio, Tampere University of Technology; *IEEE Computer,* 6/94, p. 71, 6 pp.

Processors

PowerPC 601 and Alpha 21064: a tale of two RISCs. Although PowerPC and Alpha are both RISC designs, one emphasizes powerful instructions, the other high clock speed through simplicity. James E. Smith, Cray Research, Shlomo Weiss, Tel Aviv University; *IEEE Computer,* 6/94, p. 46, 13 pp.

System-on-a-chip strategy threatens old-line ASICs vendors. Motorola's FlexCore program lets the company combine forces with high-volume customers to produce application-specific versions of its processors. Jeff Child, *Computer Design,* 6/94, p. 46, 2 pp.

System Design

Unique control schemes extend battery life in portable equipment. New, more integrated microcontrollers allow portable equipment to achieve smaller size, lower weight, and longer battery life. Doug Vargha, Maxim Integrated Products; *Electronic Products,* 6/94, p. 27, 6 pp.

Ignore packaging effects at your peril. An IC package's inductance and parasitic capacitance can lead to significant noise and ground-bounce problems at high speeds. Richard A. Quinnell, *EDN,* 6/9/94, p. 47, 4 pp.

Technique eases design of high-order PLLs. Problems distributing high-frequency clocks can be solved with phase-locked loops. Fred Salvatti, White Sands Missile Range; *EDN,* 6/9/94, p. 172, 4 pp.

Good design enables hot insertion of power supplies. A little extra design effort helps select the proper connectors, prevent contact damage, avoid power-bus glitches, and balance power distribution. Mikhail Grabois, *EDN,* 6/9/94, p. 184, 2 pp.

To multiprocess or not to multiprocess? When one processor isn't enough, use these tools and techniques to stay on a reasonable schedule and budget. Dan Strassberg, *EDN,* 6/23/94, p. 64, 8 pp.

