Resources

A Hot Time at Stanford U.

Once again, heat-seeking denizens descend on Stanford University (Palo Alto, Calif.) for the sixth annual **Hot Chips** conference on August 14–16. On Sunday, the conference opens with a pair of half-day tutorials on video compression and multiprocessor systems. The next two days are packed with presentations on recent academic and commercial chips: processors, graphics, video, and system logic. The microprocessor sessions feature the PowerPC 604, Power2+, Digital's 21164, the 68060, Metaflow's Thunder SPARC, Intel's i960 J-series and P54C, and Hitachi's SH-2 core. On Monday evening, a panel of venture capitalists discuss what's hot in their eyes. Those interested in networking may attend the separate **Hot Interconnects** conference August 11–13.

Early registration (before 7/22) for the Hot Chips conference costs $160 for IEEE or ACM members, $230 for nonmembers, and $100 for students. Each half-day tutorial costs $30 for members, $45 for nonmembers, and $20 for students. For more information, contact Dr. Robert Stewart at 415.941.6699; fax 415.941.5048 or e-mail *r.stewart@compmail.com*.

Client/Server Computing Made Easy

Well, maybe easier. Software engineers and authors Dan Harkey and Robert Orfali have written the ***Essential Client/Server Survival Guide***. This 527-page tome begins by outlining a typical client/server model, then dives into detailed descriptions of the technologies and standards in this field, covering CORBA, X/Open, DCE, and SQL among others. The authors use "soapbox" sidebars to keep their opinions separate from the analysis.

The paperback book carries a list price of $24.95 and an ISBN of 0-442-01941-6. It is available in technical book stores or from the publisher, Van Nostrand Reinhold, at 800.842.3636; fax 606.525.7778.

PC Design in Silicon Valley

Technologies such as multimedia, low-power design, and PCI continue to change the way PCs are designed. The Silicon Valley PC Design Conference (SVPC), in San Jose, will cover these and other issues on July 27–29. On Wednesday, the conference focuses on multimedia, with vendor presentations on topics such as P1394 (Firewire), VESA Media Channel, JPEG, and 3D graphics. The next day focuses on portable system issues, including power management, flash memory, and PCMCIA. Friday's high-performance theme covers PCI, fast caches, and PowerPC systems. There will also be a concurrent vendor exhibition.

Registration for all three days runs $550, or $295 per day. Exhibit-only attendance goes for $25. Contact SysTech Research at 408.293.8383; fax 408.293.0901 or e-mail *majithia@sjsuvm1.bitnet*.

The Compiler's the Thing in Montreal

As pointed out by the Intel/HP alliance, future processors must exploit greater degrees of parallelism to continue to improve performance, which may change the instruction set. The international conference on **Parallel Architectures and Compiler Techniques** (PACT '94), to be held on August 23–26 in Montreal (Canada), examines the latest research in these areas and features one of HP's VLIW gurus, Bob Rau, giving his "personal opinion" on the direction of instruction-set evolution. Other researchers will present papers on multithreaded code generation, single-chip multiprocessors, branch prediction, and distributed memory. The first day of the conference includes a choice of tutorials.

The advance registration fee (by 7/31) is US$335 for the main conference and an additional US$320 for a full day of tutorials. Contact PACT '94 at 514.848.3081; fax 514.848.2802 or e-mail *herbert@ece.concordia.ca*.