THE EDITOR'S VIEW

Announcing Processors Without Chips

Before First Silicon, Product Announcements Are Risky Business

You may have noticed a distinct lack of die photos in recent issues. It isn't that we decided to stop running them; we continue to believe that they provide valuable information about chip partitioning. But a new trend has emerged: vendors are announcing their products without waiting for die photos, or even the die themselves, to be available. This strategy makes it difficult to assess new products, but at least one rule of thumb can help.

As one might expect, high-end processors have frequently debuted without die; this roster includes Sun's UltraSparc, the MIPS R10000, HP's PA-8000, and IDT's R4700. Surprisingly, embedded vendors have followed suit, with Intel's i960 H-series, AMD's superscalar 29000, Philips' 8051 XA-1, and IDT's R4650 all appearing without any chips appearing.

Announcing early has several benefits. In some cases, vendors want to demonstrate a growth path for their existing products. The i960 and 29K announcements are for high-end products that will likely have limited initial sales in any case, but their mere existence, tenuous as it is, assures current users that they will be able to upgrade their designs as needed in the future.

When a company is debuting a new product line, not just an extension of an existing one, it is often appropriate to make an early announcement. This strategy gives the market plenty of time to evaluate the new product and begin developing software or tools to support it. The XA-1 is Philips' first 16-bit 8051; the R4650 is IDT's first embedded Orion product. These strategic moves deserve a long lead time.

In other cases, vendors that have fallen behind see an early announcement as a way of appearing competitive. Sun's SPARC performance continues to lag, but the company touts UltraSparc as the solution to its performance problems—even though the chip isn't due to ship in systems until 3Q95. HP is the last of the major RISC vendors to move to 64 bits and so has revealed its first 64-bit chip more than a year ahead of system shipments.

If not handled properly, a premature announcement can cut off sales of existing products as customers wait for a new device that is not yet available, a scenario known as the Osborne effect. A key factor is price; vendors are usually safe in announcing new high-end devices if they don't provide a price, particularly if they imply that the new device will be more expensive than existing solutions. For vendors that are introducing the first product in a new line, there may not be any sales in that area to cannibalize.

A more difficult risk to manage is that of overselling the new part. Without working silicon, it is difficult to know what the actual performance of production devices will be; all the timing analysis and simulation tools available can give only an approximation of the final performance. Although overselling is an attractive short-term strategy, in the long run it can destroy the credibility of a vendor. Sun's problems with SuperSparc *(see **081505.PDF**)* gave that company a poor reputation that has only recently begun to improve.

Since SuperSparc, Sun and other vendors have become more conservative in estimating performance, and most have delivered on their claims. A bigger bugaboo has been schedule problems. Chips ranging from Pentium to the PA-7100LC have struggled to market later than first promised.

Project planning tools are not the answer to this problem. It is actually very simple to estimate the volume availability date of systems using a new microprocessor. For new designs, particularly complex ones, plan for one year between tape out (i.e., when the physical design is complete) and volume system shipments. The designs that do significantly better than this rule of thumb are usually either simple modifications of existing designs (e.g., SuperSparc-2, the R4700) or simple embedded designs like Philips' XA-1.

Based on this rule, systems using AMD's K5 are more likely to appear in 4Q95 than 3Q95, as the company claims. Sources indicate that Cyrix has only recently taped out its M1 design, putting it on about the same schedule as the K5. AMD's superscalar 29K also may be hard-pressed to meet 2Q95 production dates. Other vendors have quoted more reasonable schedules.

Chips that are announced without even taping out face the biggest schedule risk. As AMD's Mike Johnson reminded us at last month's Microprocessor Forum, "the final week before tape out usually lasts six weeks." These chips, with designs still in flux, are also at risk for not meeting goals for die size and feature set.

The R10000 and PA-8000 fall into this final category. Their vendors seem to have allowed adequate time to complete tape out, but the R10000's estimated die size is somewhat suspect at this point. Hopefully, these vendors will be able to match the PowerPC camp's stellar