Most Significant Bits

Sun Selects HyperSparc

In a surprising move, Sun has deviated from its history of spurning externally developed CPUs, announcing that it will add 100-MHz HyperSparc systems to its existing SparcStation 20 line. Currently, this line is based entirely on Sun's SuperSparc processor; HyperSparc is a product of Ross Technology, a subsidiary of Fujitsu.

The new Model HS11 is priced at $18,695 with 32M of memory, a 1G hard disk, and a 17" color monitor. This price is 15% higher than that of a similarly configured Model 61, the current top of the line. The HS11, expected to begin shipping by year end, delivers 105 SPECint92, 13% better than a 60-MHz SuperSparc. On floating-point code, the gap is greater: 21%, based on a rating of 128 SPECfp92 for the new system. These figures are not quite as good as what Ross had originally projected *(see **0806MSB.PDF**)* but still a boost from SuperSparc.

While HyperSparc gives a short-term performance advantage, the forthcoming 75-MHz SuperSparc-2 *(see **081505.PDF**)* will roughly match HyperSparc's SPEC ratings and is due to begin shipping in January, just one month after the new HS11 systems. A 90-MHz SuperSparc-2 is slated for March. So why switch horses now?

Sun has discovered that HyperSparc far outperforms SuperSparc-2 on certain applications, despite the similarity in SPEC scores. The key factor is HyperSparc's large (256K) primary data cache compared with the two-level data cache used in SuperSparc. The two-level structure, combined with inefficiencies in the MXCC cache-control chip, adds four cycles of overhead to accesses that miss SuperSparc's 16K primary cache. A similar overhead applies to accesses to main memory.

The new HyperSparc system will do well on applications with heavy floating-point components and poor cache locality. These include EDA, financial modeling, and other applications with large data sets. The company plans to market systems based on both HyperSparc and SuperSparc-2; selling both is simply a matter of swapping MBus processor modules.

Gaining a foothold at Sun, still by far the largest consumer of SPARC chips, is a big win for Ross and ensures that the company will be able to complete its next-generation HyperSparc-2. The announcement validates Sun's MBus modular design strategy, allowing it to quickly configure a new product to meet customer demand.

FirePower Announces 603, 604 Systems

FirePower Systems (Menlo Park, Calif.) has announced its first products: a family of Prep-compliant PowerPC motherboards and systems using the 603 and 604 processors. The startup, formerly known as PowerHouse *(see **0804MSB.PDF**)*, sells only to OEMs, not to end users; its first OEM, and its principal financial backer, is Canon. Canon is expected to announced end-user availability of the systems early next year. FirePower expects to announce more OEMs soon.

FirePower initially is selling motherboards and complete systems to its OEMs but expects to focus on motherboards once the market is established. This strategy lets a company such as Canon share disk drives, power supplies, and other standard components between its x86 PCs and PowerPC systems, achieving an economy of scale that will not be possible for the PowerPC systems themselves for some time.

The systems include a low-cost uniprocessor line, called the Powerized ES, that will be available using 80-MHz 603 or 100-MHz 604 processors. The Powerized MX is a line of higher-end dual-processor systems that use two 100-MHz 604 processors.

FirePower does not use system-logic chips from Motorola or IBM; instead, the company developed its own ASICs. The startup also developed the HAL (hardware abstraction layer) for NT as well as drivers for the I/O devices. The company plans to support other Prep-compliant operating systems in the future. FirePower disputes Apple's claim that porting MacOS to this platform would be difficult, and it has offered to do so within nine months if given the chance.

End-user prices must be announced by FirePower's OEMs, but the company expects fully configured systems (without monitors) to sell for less than $3,000 for the 603 ES, $3,300 for the 604 ES, and $6,000 for the dual-604 MX. These prices are similar to or slightly lower than Pentium system prices from vendors such as Dell for comparable configurations (including Ethernet, audio, and enough RAM and disk for Windows NT).

Based on estimated SPECint92 scores, the 603 box should match the performance of a 60-MHz Pentium, while the 604 systems should far outperform 90- and 100-MHz Pentium boxes. Unfortunately, no measured benchmark results are available. Application-based performance comparisons await the emergence of applications running under Windows NT on PowerPC.

For now, these systems have little value beyond being tools for software developers, but FirePower's systems will be ready and waiting as Windows NT for PowerPC—and, presumably, applications for that operating system—begin shipping next year.

IBM Customizes PowerPC for System/36

Foreshadowing the march of PowerPC into all of its general-purpose systems, IBM has developed a PowerPC product for users of System/36 minicomputers. Although IBM stopped selling those systems years ago, there are

more than 200,000 units still in use today. To move these users to more modern technology, IBM announced the AS/400 Advanced 36, which uses a customized PowerPC processor to emulate System/36 software.

The new chip was developed by a small team in Rochester (N.Y.) and does not use any circuitry from the mainstream PowerPC 600 family. It implements the full 64-bit PowerPC architecture with added instructions to handle the peculiarities of the CISC-style System/36. To reduce system cost, the chip includes two 4K caches, a DRAM controller, and a direct interface to SPD, the I/O bus used in the AS/400 line. This design helps keep the entry price of the Advanced 36 to just $12,000.

According to IBM, the new system delivers four to eight times the performance of the fastest System/36 when executing old binaries. Next year, the company plans to introduce new software to allow the system to run both AS/400 and System/36 applications simultaneously, letting users migrate easily to the AS/400. Big Blue plans to introduce additional PowerPC-based AS/400s next year, but these systems will use a different CPU. To facilitate emulation, the AS/400 line will continue to use custom chips rather than standard PowerPC processors, at least in the near future.

Court Allows AMD to Continue 486 Shipments

Eliminating the threat of a three-month hiatus in AMD's shipments, Judge Patricia Trumbull has denied Intel's request for a temporary restraining order suspending all of AMD's 486 processor shipments. The judge instead issued a limited preliminary injunction following terms negotiated by the two companies.

Although Intel claimed to be pleased with the outcome, the company failed in its attempt to block AMD from shipping its existing inventory of 486 microprocessors that include Intel's ICE microcode but do not make any use of this code *(see **0814MSB.PDF**)*. The injunction places four restrictions on AMD:

- No new wafers with the ICE microcode can be started.
- No chips that have the system-management mode (SMM) signals bonded out (and therefore make use of the ICE microcode) can be shipped.
- After 1/15/95, no chips with ICE microcode—whether SMM signals are bonded out or not—can be shipped.
- No chips with ICE microcode can be shipped to customers that do not have existing orders or contracts.

Prior to this ruling, AMD had already switched all its new wafer starts to a design that doesn't use the ICE microcode and had taken the versions with SMM off the market, so the first two items don't change AMD's plans. AMD's inability to ship the SMM chips (486SXL and SXLV) will affect two unnamed customers and require AMD to destroy about 100,000 chips in inventory.

Chips from the ICE-free wafers now in process should be ready to ship in January, so the 1/15 deadline likewise does not affect the company—unless there turns out to be some problem with the revised chips.

The final stipulation is the only one that could cause some loss of business. Fortunately for AMD, the company has been essentially production-limited, so its current orders and contracts will probably come close to using up all of the ICE-tainted chips.

Intel to Offer DSP Software for Pentium

Working together, Spectron Microsystems (Santa Barbara, Calif.) and Intel are developing a version of Spectron's Spox operating system for the Pentium processor. Spox is a popular DSP operating system that so far runs on several DSP chips but no general-purpose processors. Earlier this year, Microsoft announced its DSP Resource Manager Interface (RMI), which works with Spox (but does not require it) and provides a standard API for applications to access DSP tasks.

The goal of the RMI is to make DSP applications hardware-independent. IASpox (Intel Architecture Spox), the version of Spox for Pentium, will make it possible to perform DSP functions without a DSP chip—a mode that Intel calls Native Signal Processing (NSP).

Using NSP, the application makes calls to the RMI, just as if a DSP chip were present, and IASpox takes care of executing the DSP task on the host Pentium processor. Thus, developers of DSP applications that already work with Spox can easily convert their applications for native Pentium execution—assuming that the applications are written in C and can be recompiled.

Spectron will offer a software development kit for IASpox to support DSP software developers in early 1995; in the second quarter, Intel will follow with technology kits to help PC system vendors implement NSP.

Intel expects IASpox first to enable PCs to produce higher-quality audio without add-in hardware. Eventually, it could be used for modems, text-to-speech conversion, voice recognition, and other audio functions. DSP performance will scale with the host CPU performance, so future systems using P6 or 150-MHz Pentium processors will enable more demanding DSP tasks to be implemented with NSP.

The emergence of IASpox threatens DSP chip makers, which have been trying for years to get their chips into high-volume PCs. Having a separate processor for DSP functions avoids the problem of sharing one processor among user-interface and time-critical tasks. But the zero hardware cost of the IASpox approach, combined with the rapid movement of Pentium systems into the mainstream, could put another roadblock in front of the DSP chip vendors.

For high-end applications, or for systems with 486 processors, DSP chips remain the best solution. But with 486 system sales expected to decline next year, the window for these DSP vendors may be shrinking. ♦

