Most Significant Bits

PowerPC Sets New Performance Targets

Launching a quick response to Intel's P6 announcement *(see **090201.PDF**)*, IBM and Motorola rolled out a vaporous plan to meet and exceed P6 performance over the next year or so. After announcing performance targets for future spins of each of the five current PowerPC chips, the partners did not explain how they will achieve these goals or when these faster parts would appear in systems, except to say that all would be shipping or sampling by the end of this year.

Figure 1 (see below) shows our projection of future PowerPC performance based on this announcement. Little has changed from the last time we published this roadmap *(see **081402.PDF**)*. We foresee a shrink version of the 603e around mid-96. This version will be built in the 0.5-micron CMOS-5X process, boosting performance to roughly 160 SPECint92 at 150 MHz.

We expect that the 604, in CMOS-5X, will also hit 150 MHz, producing about 225 SPECint92. This "604v" should exceed the performance of a 133-MHz P6 at a much lower cost. The 604v could be shipping by 4Q95, matching the performance of the 133-MHz 620.

The 620 is also due to move to CMOS-5X, jumping to about 200 MHz and 330 SPECint92. This version probably won't be ready until mid-96, however, matching it against second-generation P6 parts that should also reach about 200 MHz. Thus, the 620 should maintain a small (15–20%) performance edge over the P6.

The figure does not show the 601 and 602 lines, each of which should receive a small kicker this year. The 601 is currently available at speeds up to 110 MHz, although only Apple has access to the fastest parts. IBM intends to make 120-MHz parts generally available later this year, probably in 2Q95. These parts will continue to use the CMOS-5X process. Finally, the 602, announced at 66 MHz *(see **090203.PDF**)*, should have no problem reaching 80 MHz in its current CMOS-5L process.

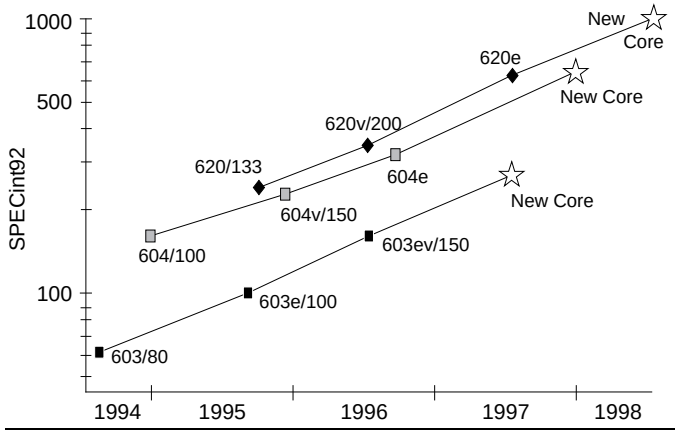

Figure 1. Projected roadmap of PowerPC processors shows continued growth along three main desktop lines. "e" indicates enhanced core; "v" indicates 2.5-V (CMOS-5X) version. (Source: MDR)

IBM has been producing 601 chips in CMOS-5X for months, so the delays in moving the other family members to this advanced process seem to come from Motorola's side. Moving the entire PowerPC line to the 0.5-micron process will offer a significant speed increase and should reduce manufacturing cost as well. The 604v is needed to compete against Intel's P6, which is due to ship this fall. The partners, however, are still struggling to deliver the initial 604, which is nominally in production but has yet to appear in any announced systems from IBM or Apple.

Even with the projected speed increase, the 620 continues to disappoint, failing to open a significant performance gap over Intel's line. Unless Intel slips up, it looks like PowerPC will lack a truly fast chip to incite power-hungry PC users to switch architectures.

MIPS Extends Its Roadmap

Not to be left out of the roadmap race, MIPS Technologies (MTI) disclosed new information about its future product plans. The plan shows that the company has now completely transitioned to a multiline model similar to PowerPC's. A high-end line will be anchored by the R10000 and follow-ons, with a midrange line consisting of follow-ons to the R4600 (Orion) family. The low end starts with the R4200.

To help with this expansion of products, MTI has called in the cavalry: Quantum Effect Design (QED), which designed Orion. Silicon Graphics (SGI), the parent of MTI, originally hoped that the R4200 would match the performance of the R4600, but SGI has now wholeheartedly embraced the speedy Orion, basing its entire Indy workstation line on QED's design. The system vendor has directed MTI and QED to work together on the follow-on to Orion, a project known as the P4.

According to the plan, the P4 is set for shipments in 2Q96 with a SPECint92 rating of 200, 50% more than the fastest current Orion chip. Given SGI's interests, the chip will receive more attention on the floating-point side than did Orion; the plan calls for tripling performance to 300 SPECfp92. This performance requires a superscalar CPU operating at 200 MHz. Yet the company plans to hold the die size to about 80 mm^2, roughly the same as Orion, using 0.35-micron technology.

Orion was designed for the Windows NT market, as evidenced by its limited FP performance. The P4 specifications are instead driven by SGI's need for a strong midrange workstation processor, a signal that the MIPS partners are losing interest in the NT market.

In 1998, the P4 will be succeeded by the D2, set to

deliver R10000-level performance while retaining the Orion cost structure. MTI expects to design the D2 without help from QED, regaining control of the midrange.

At the high end, the R8000 will receive a frequency kicker this summer through a shrink to 0.5-micron CMOS, boosting the clock speed to roughly 100 MHz. This product will be obsoleted by the R10000 *(see **081403.PDF**)*, which is due to tape out by the time you read this and make volume shipments in 1Q96.

The R10000 will initially ship in 0.5-micron CMOS with a target speed of 200 MHz; a 0.35-micron version is due in 2H96, pushing the clock speed to nearly 300 MHz. The latter version could deliver 500 SPECint92. MTI is already working on the H1, which aims to deliver 1,000 SPECint92 in 1H98.

At the low end, which for MIPS means fast consumer products rather than desktop systems, MTI plans to ship an R4200 follow-on this fall. This chip, the C1, will use a 0.5-micron process to push clock speeds above 100 MHz while shrinking the die size below 45 mm^2. In addition, the traditional SysAD bus will be replaced by a simpler 32-bit system bus. The C1 will include a faster integer multiplier, improving multimedia performance. Nintendo will probably use this part, or a similar one, in its 64-bit game system *(see **0712MSB.PDF**)*.

This plethora of products demonstrates significant investment from the MIPS partners. SGI is clearly in the driver's seat, however: the two main focus areas are workstations and set-top boxes. If MTI can deliver on this plan, its processors should be very competitive in these two markets.

HP LaserJet 5 to Use First ColdFire Chip

Motorola has announced the first implementation of its ColdFire architecture, the MCF5102. At the same time, Hewlett-Packard revealed that its newest LaserJets, the 5P and 5MP, will use the 5102, displacing Intel's i960 from its lucrative position as the core of HP's market-leading LaserJet family.

The 5102 is a fairly traditional microprocessor with no integrated peripherals. The ColdFire core *(see **081405.PDF**)* is paired with a 2K instruction cache and a 1K write-back data cache. Interrupt logic, clock generation, and a JTAG test port round out the 144-lead TQFP device. The fully static design is fabricated in 0.6-micron three-layer-metal CMOS and dissipates about 600 mW. Stated Dhrystone performance is 27 MIPS at 25 MHz. Availability is immediate at 16, 20, and 25 MHz. The 16-MHz part carries a 10,000-unit price of $19.95.

The HP design win is a huge coup for Motorola, which has been on a long losing streak in the laser-printer market after a strong initial showing. Printers from Canon and Brother as well as HP's LaserJet 4L, among others, still rely on the 68000. But HP's highest-volume units—the LaserJet 4P and 4M—use a variety of 960 chips. In fact, the LaserJet 4 consumes more than one-third of Intel's 960 shipments. HP expects these printers to be superceded by the new LaserJet 5 products.

Among the attractions leading to the selection of the 5102 were the chip's performance in PostScript processing, which is about triple that of a 960KA, and its multiplexed 32-bit bus, which reduces the routing requirements to HP's printer ASIC and allows the entire controller to be implemented on a two-layer PC board.

ColdFire's goal is to bring 68K price/performance to par with RISC chips such as the 960. The first implementation meets this goal, as HP's interest shows. HP, which already uses three other instruction sets in its various printers, was not fazed by the need to recode its algorithms for ColdFire. Motorola's newest architecture should offer stiff competition to other embedded RISCs, including its own PowerPC line.

The 960, in contrast, is seriously wounded by the loss of HP's volumes. Combined with the 960's poor prospects in hot consumer markets, this loss will further slow the growth of 960 volume, which is already lagging the rest of the market. Intel's close relationship with HP was apparently not enough to save the day for the 960.

NexGen Drops 586 Price to $239

Responding to Intel's aggressive price cuts *(see **0902MSB.PDF**)*, NexGen has slashed the price of its 586 processors by an average of 25%. In addition, the Milpitas (Calif.) company has published 1,000-piece list prices for the first time, allowing direct comparison between 586 and Pentium prices. As the following table shows, NexGen is offering 15–27% lower prices for similar integer performance levels.

NexGen CPU	Price	Intel CPU	Price	Diff
93-MHz Nx586-P100	$569	100-MHz Pentium	$673	15%
84-MHz Nx586-P90	$399	90-MHz Pentium	$546	27%
75-MHz Nx586-P80	$269	n/a	n/a	n/a
70-MHz Nx586-P75	$239	75-MHz Pentium	$301	21%

This price differential is appealing, but 586 users must purchase system-logic chip sets from NexGen, as the processor is not pin-compatible with Pentium. NexGen currently has only a single, VL-Bus chip set available, although a PCI chip set is currently in development. In addition, the 586 does not include a floating-point unit, as Pentium does. So far, several dozen third-tier vendors have adopted the 586; NexGen expects to announce some major design wins later this year.

The company reports that it is receiving significant quantities of chips in all speed grades from its foundry, IBM. Although IBM has significant capacity to devote to the 586, NexGen has even bigger plans; it expects to announce a second foundry later this year to address "future demand requirements."

NEC Cuts PA-RISC Deal

Like several other Japanese vendors, NEC is hedging its bets in the architecture wars. A maker of MIPS processors and systems, the company has inked a deal to resell more than $100 million worth of high-end PA-RISC systems over the next three years. These systems will be sold primarily in Japan.

As one of the world's largest mainframe vendors, NEC has been under pressure to offer a lower-cost alternative in the face of mainframe-downsizing products from HP, Sun, and others *(see **090301.PDF**)*. The PA-RISC systems allow NEC customers to move to a RISC-based alternative without changing vendors. Apparently, NEC was not satisfied with MIPS-based mainframe-class solutions from Tandem and others.

The Japanese vendor has no immediate plans to abandon the MIPS architecture. Instead, NEC will port some of HP's software to its midrange MIPS-based servers and port some MIPS software to PA-RISC. This cross-development could allow the company to unify its platforms in the future, if it desires.

This deal has no specific ties to the HP-Intel partnership announced last year *(see **080801.PDF**)*. But we see NEC's acceptance of PA-RISC at this late date as an implicit endorsement of the Intel-HP plan, as the company probably wouldn't commit to an orphan architecture without buying into the transition plan.

Galileo Introduces Orion Cache Controller

Startup Galileo Technology (San Jose, Calif.) has introduced the first standalone cache controller for the Orion family of MIPS processors. The GT-64012 connects directly to the system bus of an R4600 or R4700 processor, providing a write-through cache without any other system redesign. The new chip supports up to 512K of cache with zero wait states on a 50-MHz bus. At this speed, 12-ns synchronous SRAMs are required.

Galileo is a fabless vendor of system logic and specialty memory chips. It is managed by Manuel Alba, formerly of IDT, and employs a design team located in Karmiel, Israel. The company is also developing a single-chip PCI bridge for Orion processors.

The GT-64012 is currently sampling, with volume production due in 2Q95. In a 44-pin PLCC, the chip lists for $22.50 in 10,000-unit quantities. The company also sells an evaluation module—containing the 64012, tag RAMs, and 512K of cache—that plugs into an Orion CPU socket. This module allows easy prototyping and sells for $995 in unit quantities.

Although no other vendor sells a standalone cache controller for R4x00 processors, the market for complete system-logic solutions is crowded. The 64012 is compelling for embedded applications (such as networking) that don't require PC-type features but can use the extra performance delivered by a secondary cache. While other vendors focus on the small market for MIPS-based PCs, Galileo should find easier going in the expanding market for high-end embedded products.

Errata: P6 Instruction Decode

Because of incorrect information from Intel, we reported that P6 uops use a load/store model *(see **090202.PDF**)*. Actually, uops can load ALU operands from memory, increasing the flexibility of the "restricted" instruction decoders and reducing the amount of compiler optimization required. Also, the die overlay appears not to match the photo; the overlay was provided by Intel. ♦

