Patent Watch

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently:

5,416,913
Method and apparatus for dependency checking in a multipipelined microprocessor
Issued: May 16, 1995
Inventors: Edward T. Grochowski, et al
Assignee: Intel
Filed : October 3, 1994
Claims: 3
In a superscalar processor capable of executing two integer instructions in parallel, an array of comparators is provided to check for all combinations of register dependency between a pair of sequential program instructions. Additional logic is provided to validate the register fields of the instructions. If no impermissible dependencies are detected and all register fields are valid, the instructions are issued and executed in parallel. Otherwise, the instructions are executed sequentially.

5,414,822
Method and apparatus for branch prediction using branch prediction table …
Issued: May 9, 1995
Inventors: Mitsuo Saito, et al
Assignee: Toshiba
Filed: April 3, 1992
Claims: 21
Branch prediction using a table formed by an associative memory which is applicable to a superscalar processor. The branch prediction uses a table for registering entries, each entry including a branching address, a branch target address, and an instruction position indicating a position of the predicted branch instruction in a group of instructions to be executed concurrently, or an entry address indicating the position of each entry in the associative memory of the table. The correctness of the prediction is checked by using the actual branch target address and/or actual instruction position of the branch encountered in the actual execution of fetched instructions. When the predicted branch instruction is incorrect, instructions fetched subsequently are invalidated and the entry in the table is rewritten.

5,414,380
Integrated circuit with an active-level configurable and method therefore
Issued: May 9,1995
Inventors: Jeffery A. Floyd, et al
Assignee: Motorola
Filed: April 19, 1993
Claims: 20
An integrated circuit configures the active level of an input, output, or input/output pin by sensing a logic state on the pin at the inactivation of a reset signal, such as a power-on reset signal. The integrated circuit selects a true or complement signal to provide to or from an internal circuit. The voltage level on the pin is latched on the active-to-inactive transition of the power-on reset signal. Thus, the use of proper board-level termination resistors programs the pins to the desired active logic level without the need for additional logic circuitry or a dedicated device pin.

5,412,785
Microprogrammed data processor which includes a microsequencer in which a next microaddress output of a microROM is connected to the OR-plane of an entry PLA
Issued: May 2, 1995
Inventors: Robert J. Skruhak, et al
Assignee: Motorola
Filed: March 26, 1993
Claim: 1
A data processor microsequencer having a nonmultiplexed internal address bus is provided. The microsequencer includes a nanoROM for providing control information to an execution unit, an entry-point PLA for decoding a macroinstruction address and providing an initial microinstruction address, and a microROM for providing the next microinstruction address during instruction sequencing. The entry PLA accesses macroinstructions from an instruction pipeline and decodes the macroinstructions, thereby providing an initial microinstruction address for the microroutine to perform the macroinstruction.

The initial microinstruction address is temporarily stored in a microprogram counter latch (uPC) and provided to the microROM or the nanoROM for decoding. The microROM decodes the initial microinstruction address and provides N output bits that are routed directly into the PLA and subsequently provided to the uPC. The uPC selectively transfers the next microaddress to the microROM, and the microROM decodes the next microaddress, thereby providing subsequent microaddresses in the microroutine directly to the PLA.

Other Issued Patents
5,414,820 *Crossing transfers for maximizing the effective bandwidth in a dual-bus architecture*
5,414,824 *Apparatus and method for accessing a split line in a high-speed cache* ♦

