GEC Plessey Spins New ARM Chips

Butterfly, Spider, and Mantis Targeted at Portable Communications

by James L. Turley

Following the lead of other ARM licensees, GEC Plessey has developed three new microcontrollers based on the ARM7 core. Each of the new devices combines a mixture of serial I/O, DMA, and a PCMCIA interface to create low-cost intelligent controllers for portable communications-oriented products.

The three new chips, courageously named Butterfly, Spider, and Mantis (they have no traditional part numbers), should find homes in small battery-powered communications devices like cellular telephones, PCMCIA modems, and portable LAN adapters. Although their 32-bit cores and low prices make for attractive price/performance ratios, hardware limitations in the design will drastically reduce the available performance that designers can get.

GEC Plessey Strikes Out on Its Own

GEC Plessey Semiconductors (GPS) has shipped the lion's share of ARM-based microprocessors in the past few years. The Swindon, U.K.-based company provides ARM60 chips to Matsushita for its 3DO Multi-Player and produces the majority of ARM610 chips going into Apple's Newton.

Identical versions of those processors are available from other vendors. The Butterfly, Spider, and Mantis chips are the company's first foray into original design and its first move toward differentiating itself from the rest of the ARM pack. All three chips capitalize on GPS's experience in developing mixed-signal, communications, and RF components for its European customers.

	Butterfly	Spider	Mantis
Frequency (3.3 V)	15 MHz	20 MHz	20 MHz
Frequency (5 V)	25 MHz	30 MHz	30 MHz
Data bus	32 bits	16 bits	32 bits
Address bus	22 bits	20 bits	22 bits
PCMCIA	No	Yes	Yes
UARTs	2	1	2
DMA channels	None	2	2
Timer/counter	4	4	4
Watchdog	Yes	Yes	Yes
Parallel I/O	8 bits	None	16 bits
Die size	30 mm^2	32 mm^2	56 mm^2
Process	0.7µ, 3M	0.7µ, 3M	0.7µ, 3M
Package	PQFP-144	PQFP-144	PQFP-208
Est mfg cost*	$7	$8	$14
Price (10K)	$18	$25	$34

Table 1. The three ARM-based controllers from GEC Plessey share most features, differing mainly in the mix of peripherals on each chip. (Source: GPS except *MDR estimates)

Three New Chips Take Wing

The three devices are very similar and are effectively subsets or supersets of one another. They have identical ARM7 cores, a built-in SRAM/ROM controller, a set of four 32-bit timers, and at least one UART. As Table 1 shows, the difference among the parts is simply the mixture and number of the remaining peripherals.

Butterfly is the smallest and least expensive member in this new phylum. Its core runs a bit slower than the other two chips, and it has no DMA controller. The middle chip, Spider, pulls off Butterfly's parallel I/O, one UART, and half its data bus in exchange for a PCMCIA interface, so as to fit in the same PQFP-144 package.

The third chip, Mantis, essentially combines the features of the other two. It has all the features of Spider plus a second serial port, a pair of 8-bit parallel ports, external enable pins for two of its timers, and wider address and data buses. Looked at another way, Mantis is similar to Butterfly but adds a PCMCIA interface, DMA controller, and second parallel port. The increased number of I/Os requires a larger package, so Mantis has 208 legs, versus 144 for Spider and Butterfly.

As Figure 1 shows, both Spider and Mantis have a PCMCIA slave interface that conforms to version 2.1 of the standard. The interface allows both 8- and 16-bit transfers to and from a host system. A 16C450-compatible UART is included as part of the interface logic, to appease DOS systems expecting PC-compatible hardware.

The PCMCIA interface supports only slave transactions, forcing Spider and Mantis into roles as peripherals rather than as small microcontrollers that could use PCMCIA cards for memory or I/O expansion.

Although these chips are targeted at communications applications, they include only simple UARTs. All UART channels are identical and support basic five-wire RS-232-type interfaces with transmit, receive, CTS, RTS, and DCD handshake signals. The UARTs can be polled or can generate interrupts; they have a maximum bit rate of 400 Kbps.

Lack of Cache Squashes Performance

None of the chips has any cache or on-chip memory. The ARM7 core is forced to fetch instructions from external memory through its on-chip memory controller. ARM's fixed 32-bit instructions and single-cycle execution place heavy demands on the external memory. In

the case of Spider in particular, which has only a 16-bit bus to memory, this exacts a serious toll. All three of these chips would have benefited from the Thumb core *(see **090401.PDF**)* but were developed too early.

At 25 MHz, the chips have only 40 ns to access external SRAM; allowing for 15 ns of logic delay and setup time, 25-ns SRAMs are required to achieve peak performance. Such chips are expensive—hardly in keeping with the goal of enabling low-cost portable peripherals. Choosing less budget-busting 65-ns SRAMs slashes peak performance by half.

ARM cores, like many RISC processors, are exquisitely sensitive to instruction-fetching delays. The core consumes one 32-bit instruction per clock; without a cache, these instructions must come from external RAM or ROM. Adding a single extra clock cycle to the chips' memory latency cuts performance directly in half. Additional delays decrease performance proportionally.

The bigger issue is bandwidth. An ARM chip without a cache needs a 32-bit instruction every cycle, saturating its single-cycle external bus. Every data access forces an instruction fetch to wait, causing a pipeline stall. Even in an ideal system, then, Butterfly and Mantis could deliver only about 80% of the best-case performance of their respective cores. Spider, with its narrow bus, fares much worse, yielding less than 40% of peak performance.

ARM Core Gives Chips a Leg Up

These chips' small size, moderate performance, and modest power consumption make them interesting new alternatives for PCMCIA communications cards. Lacking the PCMCIA interface logic, Butterfly is obviously left out of this market, but it could be used in noncomputer applications, like cellular phones or as an intelligent serial controller on the motherboard of a small PDA. In such products, the PWM output from its timer could control the brightness of an LCD screen or drive simple beeps out of a piezoelectric speaker.

In features and applications, the three GPS parts are similar to Motorola's 68PM302 *(see **090502.PDF**)* or the 68340/41. They all integrate a 32-bit microprocessor core with serial-control peripherals, timers, and (in the case of the 'PM302) a PCMCIA slave interface. Motorola has priced the 68PM302 at about $17 in quantity, undercutting even the $18 Butterfly chip. The '302 also includes more advanced serial communications hardware than the basic UARTs found in any of the new ARM offerings from GPS.

The biggest difference is in the core performance. Spider and the others can spin webs around any of the 68300-family devices in all but the worst situations. Motorola's 68EC000-based '302 chips can muster perhaps 2–3 Dhrystone MIPS at 20 MHz (the 68PM302's top speed) compared with nearly 20 MIPS for a Butterfly or Mantis chip with fast enough memory. Spider will achieve approximately half that rate. The 68340 and '341, which are based on a faster CPU32+ core, peak at 5–6 Dhrystone MIPS.

Operating power dissipation is not wildly different between the two vendors' devices. Both dissipate less than half a watt during typical full-speed operation. In standby mode, however, Mantis burns two orders of magnitude less energy: 5 µW (typical) versus 68PM302's 500 µW. Keeping the '302's 1K of on-chip SRAM alive accounts for some of this difference.

Butterfly, Spider, and Mantis are interesting chips that give card designers a new alternative. The ARM core is smaller and generally more powerful than the 68K or 16-bit cores available in competing devices. If designers are careful not to overestimate the performance obtainable from these devices, they should make a nice addition to many PCMCIA cards. ♦

Price & Availability

Butterfly is in production now; in 10,000-unit quantities, the chip is priced at $18 in a PQFP-144 package. Spider and Mantis will both begin sampling in October with production scheduled for December. In lots of 10,000, Spider is priced at $25 in a 144-lead TQFP; Mantis costs $34 in a PQFP-208 package. An evaluation board is also available for $2,300. For more information, contact GEC Plessey Semiconductors (San Jose, Calif.) at 408.451.4700; fax 408.451.4710. Or contact GEC Plessey (Swindon, U.K.) at 44.1793.518.000; fax 44.1793.518.411.

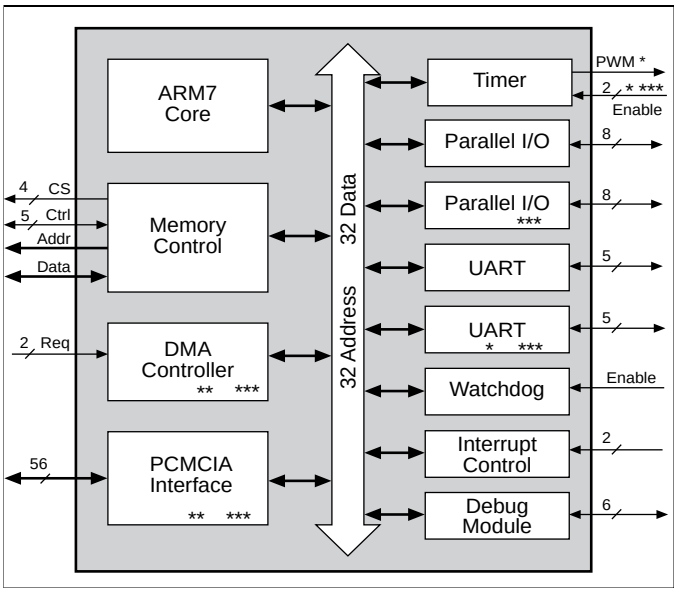

Figure 1. All three GPS controllers share the same core but have different peripherals on the chip's internal bus. The memory controller handles SRAM or ROMs. *Butterfly only; **Spider only; ***Mantis only.

