Literature Watch

ASICs

Behavioral synthesis yet to prove itself beyond DSP. If behavioral synthesis is to have a chance at catching on as a mainstream technology, we have to examine current HDLs, push for synthesis standards, and develop formal verification methods. *Computer Design,* 6/95, p. 88, 6 pp.

Optimizing the layout of deep-submicron designs. Deep-submicron physical effects dramatically increase the importance of layout optimization relative to logic optimization. These effects make physical floorplanning and timing-driven layout critical steps in the design process. Erach Desai, ArcSys; *Computer Design,* 6/95, p. 98, 3 pp.

Buses

Bus-switching chip busts bandwidth barriers. I-Cube's PS family of programmable switching devices provides building blocks for crossbar buses. Jeff Child, *Computer Design,* 6/95, p. 32, 4 pp.

Development Tools

Standards groups vow to solve tool interoperability problems. Sematech, CFI, and EDAC are developing an EDA standards roadmap to coordinate EDA tools from multiple vendors. Mike Donlin, *Computer Design,* 6/95, p. 44, 2 pp.

Windows-based EDA tools attack the UNIX old guard. For years, UNIX-based EDA tools have dominated the world of sophisticated PCB design. But increasing PC compute power and the popularity of Windows software might finally be threatening the UNIX powerhouses in the design-tool arena. Mike Donlin, *Computer Design,* 6/95, p. 57, 9 pp.

Graphics/Video

Multimedia IC integrates 3D, video and sound. Nvidia's NV1 delivers the graphics and sound capabilities of a high-end game machine to PC users. Tom Williams, *Computer Design,* 6/95, p. 48, 2 pp.

Single chip handles audio/video multimedia. Nvidia's NV1 simplifies system design by combining audio and 3D video in one chip. Dave Bursky, *Electronic Design,* 5/30/95, p. 139, 3 pp.

Memory

Flash-memory choices boost performance and flexibility. Higher density flash memories and innovative memory architectures give designers more freedom. Dave Bursky, *Electronic Design,* 5/30/95, p. 63, 7 pp.

Flash memory mutates as it moves to higher densities. Dataquest projects 16-Mbit flash-memory shipments to grow from about 15 million in 1994 to more than 100 million in 1998. Jeff Child, *Computer Design,* 6/95, p. 119, 3 pp.

A thumbnail sketch of cache memory. Synchronous SRAMs are becoming more popular as their prices continue to drop. Markus Levy, *EDN,* 5/95, p. 16, 4 pp.

Miscellaneous

Ball grid arrays: the next surface-mount package of choice. Both ceramic and low-cost plastic packages meet performance and density needs for housing high-pin-count chips. Jon Houghton, Motorola; *Electronic Products,* 6/95, p. 33, 4 pp.

More pins and less space beget new IC packaging. As pin count grows, new packages are emerging, including BGA, µBGA, TAB, MCM, and VSPA. Dan Strassberg, *EDN,* 5/25/95, p. 61, 7 pp.

Processors

In µPs, smaller is sometimes better. CPUs grab the glory, but microcontrollers outsell them by orders of magnitude. Jack Ganssle, *EDN,* 5/25/95, p. 167, 2 pp.

A general-purpose fuzzy inference processor. Siemens' SAE 81C99 processor supports a maximum inference speed of 10 million rules/s at 20 MHz. Herbert Eichfeld, Martin Klimke, et al, Siemens AG; *IEEE Micro,* 6/95, p. 12, 6 pp.

Implementation trade-offs in using a restricted data flow architecture. This ISCA '95 paper analyzes the design of Hal's Sparc64 CPU. M. Simone, A. Essen, et al, Hal Computer; *Computer Architecture News,* 5/95, p. 151, 12 pp.

Performance evaluation of the PowerPC 620 microarchitecture. This ISCA '95 paper presents an instruction-level performance evaluation of the 620 CPU. Trung A. Diep, Christopher Nelson, et al, Carnegie Mellon University; *Computer Architecture News,* 5/95, p. 163, 11 pp.

A comparative analysis of schemes for correlated branch prediction. This ISCA '95 paper compares a wide variety of static and dynamic algorithms. Cliff Young, Nicolas Gloy, et al, Harvard; *Computer Architecture News,* 5/95, p. 276, 11 pp.

Multiscalar processors. This ISCA '95 paper describes a processor with multiple program counters, many function units, and a single logical register file. Gurindar S. Sohi, Scott E. Breach, et al, University of Wisconsin; *Computer Architecture News,* 5/95, p. 414, 12 pp.

System Design

Integrating Alpha, VMEbus, and apps. Matching a fast embedded processor to a mature bus technology calls for creative hardware and software solutions. Mark Bronson, Aeon Systems; *Electronic Design,* 5/30/95, p. 126, 4 pp.

Effective cache prefetching on bus-based multiprocessors. Victim caching and compiler-based restructuring of shared data make prefetching effective for a wide range of system designs. Dean M. Tullsen and Susan J. Eggers, University of Washington; *ACM Transactions on Computer Systems,* 2/95, p. 57, 32 pp.

Set-associative cache simulation using generalized binomial trees. This article proposes an efficient technique for simulating a group of set-associative caches in a single pass. Rabin A. Sugumar, Cray Research, et al; *ACM Transactions on Computer Systems,* 2/95, p. 32, 25 pp.

