# Most Significant Bits

**Intel Sues UMC to Block 486**

Just over a year after United Microelectronics Corp. (UMC) announced its 486SX microprocessor *(see **090701.PDF**)*, Intel has filed patent infringement suits against the Taiwan-based company in Singapore, Hong Kong, Germany, and the United Kingdom. UMC has been shipping 486SX-compatible chips, serving the low end of the market, and the company recently demonstrated 486DX and DX2 processors. Intel is seeking to stop shipments of the allegedly infringing chips, but an Intel spokesperson said that what Intel is really concerned about is not the 486 but a possible Pentium-class follow-on, which UMC has promised for 1996.

UMC has stated that it believes its design does not infringe any Intel patents, and that some Intel patents are invalid due to prior art. If the litigation against UMC goes to trial, it will be the first time that the validity of Intel's x86-related patents, as well as the possibility of creating a compatible design that does not infringe them, is challenged in court.

Intel did not file its action in the U.S. because UMC does not sell its chips in this country and has instructed its customers not to ship systems with UMC chips to the U.S. An Intel spokesperson said that Intel did not file suit in Taiwan and France because UMC has already initiated legal action in those countries. The UMC action is different, however, in that it deals only with the equivalent of the "Crawford" ('338) memory-management patent, which UMC is seeking to invalidate on the basis of prior art. Intel may have focused its legal efforts in countries where UMC would have the most difficulty defending them. Intel has left the Crawford patent out of its claims against UMC, possibly reflecting concern over the strength of that patent.

The German suit cites patent DE3,618,163 and names UMC's Netherlands sales office and a distributor. The other suits name the local UMC sales offices and distributors and cite U.K. patents 2,059,124 (Extended Address Single and Multiple Byte Microprocessor), 2,229,832B (Byte Swap Instruction for Memory Format Conversion Within a Microprocessor), and 2,230,118B (Microprocessor Providing Selectable Alignment Checking on Memory References).

The first of these U.K. patents is equivalent to U.S. patents 4,449,184 and 4,363,091, which are 8086-related and cover the segmented MMU and the instruction queue, respectively. The other two U.K. patents do not appear to have U.S. equivalents; they cover the 486's byte swap instruction and the ability to generate an interrupt on a misaligned memory reference.

Some of these issues were raised in Intel's patent infringement suits against Cyrix and Chips and Technologies. The Cyrix litigation never reached the infringement issues because Cyrix prevailed in its claim that its foundries' licenses cover the chips. C&T reached an out-of-court settlement with Intel, presumably enabled by the fact that C&T dropped out of the processor market.

**Data General Drops 88000 for P6**

Becoming the biggest computer vendor to switch from RISC back to CISC, Data General has announced that it will use the P6 processor in a future line of servers, eventually replacing its 88000-based Aviion line. These new systems are expected in 1H96. The company will port its DG-UX operating system to the x86 architecture to ease its customers through this transition.

The company recently announced plans to port DG-UX to SPARC as well *(see **090703.PDF**)*, but the new announcement indicates that x86 will be the company's strategic direction in the future. The SPARC port may serve the needs of high-end customers that need more performance than the P6 can provide.

The move follows Intergraph's decision to drop its Clipper architecture in favor of Pentium-based workstations. While Intergraph was drawn by the floating-point improvements in Pentium, Intel's addition of a high-bandwidth server bus to the P6 helped attract Data General. Both companies presumably hope to tap the vast infrastructure of x86-compatible hardware and software to lower the cost of their products.

**Cirrus Chip Set Targets "Super" 486s**

PicoPower Technology, now a subsidiary of Cirrus Logic, has announced the Sequoia family of system-logic chip sets. Although it may seem late in the game to target the 486, Sequoia is designed to support high-end processors that use a 486 bus, including AMD's fast 486DX4 parts *(see **0908MSB.PDF**)* and Cyrix's new 5x86 *(see **090901.PDF**)*. These processors will be popular in desktop systems and particularly notebooks at least through the middle of next year.

While many 486 chip sets limit the processor-bus speed to 33 MHz, Sequoia supports speeds of up to 50 MHz. AMD's 120-MHz 486DX4, for example, requires a 40-MHz bus, and we expect AMD to eventually deliver 150-MHz parts, pushing a chip set like Sequoia to its limit. The 100-MHz 5x86 requires a 50-MHz bus for maximum performance. Sequoia supports the write-back L1 caches used by these processors as well as zero-wait-state L2 caches and interleaved EDO DRAM for main memory, all of which improve system performance.

Sequoia also includes an "instant-on" capability. Instead of turning off a Sequoia-based desktop PC when it is not in use, the user can let it go into a deep sleep

 

mode, consuming only a few watts of power. From this mode, the user can quickly return to full operation with a single keystroke. The system can also power up in response to an incoming fax or telephone call, making it ideal for a home user. PicoPower's traditional power management is also provided for mobile systems.

The Sequoia set consists of two chips and is available in three package options: 160-pin PQFPs for desktop systems, 176-pin TQFPs for notebooks, and 144-pin TQFPs for embedded applications. (The last option omits the L2-cache interface and allows fewer ISA devices). The chip set is currently sampling at $40, with volume production planned for 3Q95. The company says the volume price will be "well under $20."

**Avance Delivers 64-Bit Graphics for $15**

It seems like yesterday that 64-bit chips were the latest in high-end graphics *(see **070901.PDF**)*. Avance Logic (Fremont, Calif.) has pushed this feature from the midrange into the low end by deploying the ALG2064 graphics accelerator for just $15. In addition to 64-bit performance, the new chip provides an integrated RAMDAC, clock generator, and 32K BIOS ROM. It connects directly to PCI or VL-Bus.

The 64-bit graphics engine provides popular GUI operations such as bitBLT, line draw, and polygon fill, but it does not include any video acceleration features. The 2064 connects to 32- and 64-bit-wide frame buffers using either fast-page-mode or EDO DRAM. The minimum frame buffer size is 1M in 32-bit mode or 2M in 64-bit mode. Since makers of low-end systems may not want to add a second megabyte of frame buffer, they may stick with a 32-bit interface for cost reasons.

The integrated clock generator produces the necessary clocks for the DRAM and RAMDAC. The 110-MHz RAMDAC supports high resolutions and refresh rates. The integrated BIOS is optimized for the 2064; it provides PCI and VL-Bus compatibility and a variety of display modes. The chip, which uses a 208-pin PQFP, also complies with the EPA Energy Star and VESA DDC (1 and 2B) standards.

Avance is now sampling the 2064 and expects it to reach volume production this month. The $15 price, in OEM quantities, and high level of integration make the device attractive for very low cost PCs. Even at this price point, the chip offers reasonable performance in a Windows environment. These low-end systems are likely to stick with a 32-bit frame buffer, however, reducing the chip's performance advantage.

Game and educational programs are making increasing use of video; for video-based software, the 2064 will not perform as well as more expensive chips. For most software, however, the 2064 will deliver solid performance at a low cost, satisfying the needs of entry-level PC users.

**S3 Delivers Multimedia Chip Set with MPEG**

S3's new multimedia chip set is the first of its kind to integrate MPEG, audio, and video functions. The three chips are a graphics/video accelerator (Trio64V+), an MPEG-1 audio/video decoder (Scenic/MX1), and an audio DAC (Sonic/AD). The set offers TV-quality video and CD-quality audio and is designed for desktop applications in the home and office.

The Trio64V+ combines graphics and video acceleration at up to $1024 \times 768 \times 16$ resolution and has a direct interface to live video and MPEG-1 peripherals. It incorporates a 135-MHz 24-bit RAMDAC and a dual-clock synthesizer. The chip supports MPEG-1, Indeo, and Cinepak video playback with arbitrary scaling, linear interpolation, and color-space conversion (YUV to RGB).

The Scenic/MX1 provides MPEG-1 video decoding at 30 frames per second, MPEG-1 audio decoding, and a serial output port for direct connection to a low-cost audio converter. Sonic/AD fills this bill, providing two 16-bit audio channels. It uses a 4× interpolation filter, a 64× sigma-delta DAC, and linear phase filtering to provide a 90 dB range with less than -80 dB typical total harmonic distortion.

The chip set also includes a glueless PCI or VL-Bus interface. Its bus-mastering capability significantly reduces the amount of CPU involvement needed for multimedia functions, although the CPU is still responsible for demultiplexing the incoming MPEG data into separate video and audio streams. S3 has developed its own software drivers for Windows 3.11, Windows NT, Windows 95, OS/2, and SCO UNIX.

The company prices the chips separately, since the MPEG-1 chip and audio DAC are optional. The Trio64V+ sells for $32, the Scenic/MX1 for $35, and the Sonic/AD chip for $3.85, all in quantities of 10,000. The chip set is now sampling, with production due later this quarter.

S3 has quickly gathered some impressive endorsements. Compaq will employ S3's chip set in future Presario PCs and bundle MPEG software from companies such as Microsoft, Creative Multimedia, IVI Publishing, and Knowledge Adventure.

These endorsements indicate the growing momentum behind the MPEG-1 standard. Packard Bell also plans to include MPEG chips in its consumer PCs by the end of this year. Given the increase in transistor budgets, we expect the next generation of graphics chips from S3 and others to combine GUI acceleration and MPEG-1 decoding onto a single chip, eliminating the expense of standalone decoder chips and offering MPEG-1 essentially for free. This backing for MPEG could spell trouble for Intel's Indeo video.

One feature that the S3 chip set lacks is 3D-graphics acceleration. Chips such as Nvidia's NV1 *(see **090904.PDF**)* and Trident's T3D2000 *(see **0909MSB.PDF**)* provide this capability at a price similar to that of the S3

 

chip set, although neither offers MPEG support. As 3D games become more popular, S3 may need to add this feature to its multimedia portfolio.

**Trident Stokes 3D Fire**

Known more for its low-cost graphics chips, Trident Microsystems (Mt. View, Calif.) has introduced a 3D accelerator for PCs. Targeted at both CAD/CAM and 3D games, the T3D2000 includes a 64-bit GUI accelerator with video and 3D-graphics acceleration. The device is scheduled for October production with an initial list price of $60 in 1,000-unit quantities.

The single-chip design provides basic GUI acceleration features and adds video features such as scaling, color-space conversion (YUV to RGB), and color dithering. The chip also accelerates typical 3D rendering operations such as Gouroud shading, texture mapping, alpha blending, and Z-buffering. Trident estimates its performance at 250,000 100-pixel Gouroud-shaded triangles per second. The company will supply drivers for the 3D DDI interface in Windows NT and Windows 95.

The T3D2000 allows a flexible system design, with a 64-bit interface to 1M–16M of memory for the frame buffer and Z-buffers. It supports DRAM, VRAM, or WRAM (window RAM), and the designer can use different types of memory for frame buffers and Z-buffers. The chip connects directly to either PCI or VL-Bus and requires an external RAMDAC.

The chip is well suited to CAD/CAM and other technical applications. The chip is relatively expensive for a PC graphics chip, however, and extra Z-buffer memory adds significantly to the system cost. Thus, T3D2000 systems will be too expensive for consumer systems running 3D games. Nvidia's multimedia chip *(see **090904.PDF**)* is tuned specifically for 3D games; by eliminating the Z-buffer, it provides a more cost-effective solution when CAD applications are not needed.

We expect other vendors to enter the 3D graphics market, taking advantage of the growing workstation-downsizing opportunity and Microsoft's support of OpenGL. Trident should gain an advantage from being one of the first to deliver a low-cost 3D accelerator. ♦

 