Patent Watch

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently:

5,414,864
Method for selectively saving/restoring first registers and bypassing second registers in register units …
Issued: May 9, 1995
Inventors: Shinobu Koizumi
Assignee: Hitachi
Filed: July 19, 1990
Claims: 8
A data-processing system having a CPU that includes a register file for storage of often-used data. A method and system is provided for saving and restoring the contents of the register file from the main memory only when necessary. Each register unit in the register file includes a register-protection flag, a save-area pointer, and general-purpose registers. The register-protection flag is coded to identify if the register unit is in actual use. Before saving or restoring the register unit, its register-protection flag is checked, and only if the flag indicates actual use is the saving or restoring performed.

5,414,848
Method and apparatus for sharing a common routine stored in a single virtual machine …
Issued: May 9, 1995
Inventors: David A. Sandage, et al
Assignee: Intel
Filed: April 1, 1993
Claims: 16
The system runs Microsoft Windows 3.1 in enhanced mode. The system memory contains a virtual machine (VM) and at least one DOS VM. A target VM contains shared-code routines for use by all VMs loaded in the computer system. When access to the shared-code routine is desired from calling process in a calling VM, the calling VM transfers control and calling data parameters to a shared-code virtual device driver (VxD). The shared-code VxD translates the calling data parameters so that the target VM can access them. The shared-code VxD invokes calls to a Windows process scheduler to schedule the target VM and block the calling VM. The target VM, upon invocation by the scheduler, executes the shared-code routine and generates return parameters.

5,414,828
Apparatus for configuring relative position of a cache memory in a cache memory array
Issued: May 9, 1995
Inventors: Eran Yarkoni, et al
Assignee: Intel
Filed: July 19, 1992
Claims: 6
A cache memory that includes a cache controller is formed on a single substrate. Multiple memories may be used in an array. The memories themselves determine how many other memories are in an array and each of their relative positions in the array. From this information, each memory sets the range of its set fields and the size of its tag fields. This is done on reset with the configuration information being distributed among the memories themselves, without being centrally stored, and in a manner transparent to the software.

5,412,798
System for enabling access to device driver residing in resource memory corresponding to coupled resource …
Inventor: John I. Garney
Assignee: Intel
Filed: January 22, 1993
Claims: 18
A card device driver is separated into two parts: a full device driver portion and a stub portion. The full device driver provides all functionality necessary to control every function of the card. The stub is a small portion of logic for linking the full driver with operating-system software. A fixed amount of system memory is set aside at bootstrap initialization to contain the stubs. Stubs corresponding to removed cards remain resident in system memory until a stub cannot be loaded because the system memory that was set aside has been filled. At that time, enough of the system memory set aside for stubs is reclaimed to permit the desired stub to be loaded. Therefore, by allocating enough space in system memory to contain every stub required by the system at a given time, and by reclaiming system memory occupied by removed card stubs as the memory is needed, one can avoid having to periodically reset the system by performing a bootstrap initialization procedure.

Other Issued Patents

5,404,483 *Processor and method for delaying the processing of cache coherency transactions during outstanding cache fills*
5,404,482 *Processor and method for preventing access to a locked memory block by recording a lock in a content-addressable memory with outstanding cache fills*
5,404,476 *Multiprocessing system having a single translation lookaside buffer with reduced processor overhead*
5,404,457 *Apparatus for managing system interrupt operations in a computing system* ♦

