New PowerPCs Aimed at Consumer Devices

IBM and Motorola Double the Number of Embedded PowerPC Chips

by Jim Turley

At a stroke, IBM and Motorola have together doubled the number of embedded PowerPC chips available. The new devices add peripheral features and boost clock speeds compared with their predecessors. While IBM has made an incremental improvement to its existing 403 chips, Motorola's move is bolder: for the first time, the company has mixed a PowerPC core with peripherals from its popular 68300 line. One of the new microprocessors is aimed at PDAs, another is tailored for data communications, while the third has already been selected for a number of television set-top box designs.

The 403GC from IBM is a minor spin on the company's existing 403GA and 403GB, but with a new MMU added. Motorola's MPC821 and MPC860 use the same PowerPC core as the earlier MPC505 but include a complex communications block taken from the company's peripheral warehouse. All three chips deliver competitive performance and keep power consumption to around half a watt, as Table 1 shows.

Motorola Chips Share Common Peripherals

The 821 and 860 are nearly identical, the major difference being the LCD controller on the 821 versus the two additional serial channels on the 860. The large communications processor block in both chips is lifted from Motorola's 68360 QUICC chip *(see **070603.PDF**)*, although it was trimmed somewhat for the 821. The communications processor itself is programmable and runs independently of the CPU, making the 821, 860, and 68360 special-purpose dual-processor systems on a chip. Thus, the 860 is compatible with drivers written for the 68360—up to a point. Programmers familiar with the communications processor can transport lower-level code between the two. Porting the operating system or application-level code from 68000 to PowerPC is another matter entirely.

There are five versions of the 860, with varying levels of serial I/O; on the most capable ones, all four SCCs support Ethernet transactions in addition to a number of other protocols. On the 821, only the first of its two SCCs supports Ethernet. For a PDA, even a single Ethernet port is exceptional. Perhaps a docking adapter or base station could provide a wired network connection and additional interface hardware.

On both new chips, the 68360's original communications processor has been upgraded with the addition of a multiply-accumulate (MAC) primitive. An intrinsic MAC function is useful for software modems and other data-conditioning tasks, benefitting both the 821 and the 860. Motorola has also pointed out the MAC's usefulness for voice recognition. Dragon Systems (Newton, Mass.), a long-time developer of voice-recognition software for PCs, is porting its code to the 821's communications processor module.

	Motorola MPC505	Motorola MPC821	Motorola MPC860	IBM 403GA	IBM 403GB	IBM 403GC
Max freq	25 MHz	40 MHz	40 MHz	33 MHz	28 MHz	33 MHz
MIPS*	46 MIPS	52 MIPS	52 MIPS	41 MIPS	35 MIPS	41 MIPS
I-cache	4K	4K	4K	2K	2K	2K
D-cache	4K RAM	4K	4K	1K	1K	1K
MMU	No	Yes	Yes	No	No	Yes
TLBs	n/a	32-entry	32-entry	n/a	n/a	64+4
FPU	Yes	No	No	No	No	No
DRAM ctrl	No	Yes	Yes	Yes	Yes	Yes
Serial	None	5 ports	7 ports	1 port	None	1 port
Parallel	None	12 bits	12 bits	None	None	None
Timers	1	1	1	4	4	4
DMA	None	None	None	4	4	4
PCMCIA	No	Yes	Yes	No	No	No
LCD control	No	Yes	No	No	No	No
Voltage	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
Power (typ)	850 mW	540 mW	540 mW	265 mW	300 mW	300 mW
Package	PQFP	BGA	BGA	PQFP	PQFP	PQFP
Pins	144	357	357	160	128	160
Price (10K)	$70	$70	$68–$122	$45	$40	$40

Table 1. The two new Motorola chips are geared for communications and personal-communicator applications, while IBM's 403GC is the company's first to have an MMU and is destined for set-top boxes. *based on Dhrystone 2.1 (Source: vendors)

The MAC function is part of the communications processor, not the PowerPC core; neither company has yet added an integer MAC instruction to its PowerPC chips, as many MIPS vendors have done.

The memory controller connects gluelessly to DRAMs, SRAMs, EPROMs, and flash memories. For DRAMs, the new chip drives four RAS, CAS, and WE lines according to user-programmable timing parameters, with one-quarter-clock resolution.

LCD Controller Sets 821 Apart

The biggest feature distinguishing the 821 from the 860 is its LCD controller, as Figure 1 shows. Similar to the one in Motorola's 68328 DragonBall chip *(see **090903.PDF**)*, the LCD controller handles

Price & Availability

The IBM 403GC is sampling now in 25- and 33-MHz speed grades. Packaged in a 160-lead PQFP, the part is priced at $44.30 in 1,000-piece quantities. Motorola's MPC821 is sampling now in a 357-contact plastic ball-grid array (PBGA) at 40 MHz. Production is scheduled for 1Q96. In 10,000-unit quantities, the 821 is priced at $70. Four versions of the MPC860, which is also in a PBGA-357 package at 25 and 40 MHz, will begin sampling in 4Q95, with production in 2Q96 (the 860MH will be one quarter later). Prices range from $68 for a 25-MHz 860DC to $122 for a 40-MHz 860MH.

For more information, contact IBM Microelectronics (Research Triangle Park, N.C.) at 800.769.3772 or Motorola (Austin, Texas) at 512.891.3823; fax 512.891.8807.

resolutions up to 1024 × 1024 and uses system memory as a frame buffer. Whereas the '328 handles only monochrome LCD panels, the 821 can do color—16 colors from a palette of 256. Both TFT (thin-film transistor) and passive color (PSTN) screens are driven directly from onboard logic.

Both new chips operate on 3.3-V supplies with 5-V–tolerant I/O. Power consumption is around 300 mW at 25 MHz. Motorola has also laid the groundwork for future low-voltage operation: the core can be fed with a separate 2.2-V supply at speeds below 25 MHz, reducing power consumption another 30%.

IBM Adds MMU to 403 Family

In a nutshell, IBM's new 403GC is simply a 403GA with an MMU. Driven by a television set-top box customer, IBM took the existing 403GA *(see **080601.PDF**)* and grafted a custom MMU onto the chip, adding about 10% to the overall size of the die. The 'GC is pin-compatible with the 'GA, and the two parts have identical clock speeds and similar power-dissipation rates. The set-top box deal has since fallen through, and IBM admits that without the customer demand, the part probably would never have been developed. Nonetheless, the 'GC now allows IBM to compete for PDAs, set-top boxes, and other applications that require an MMU.

The MMU in the 403GC is, so far, unique to that chip. It differs from the PowerPC "Book 3" specification used by the 60x desktop processors. However, it is not vastly different from the MMU in Motorola's new chips, and IBM has indicated that the design will appear again in future 40x implementations.

The MMU includes 64 fully associative TLB entries. Each TLB entry describes a page, with eight selectable page sizes starting at 1K. Small page sizes are good for embedded systems, where data and code blocks tend to be smaller than for desktops.

TLB replacement is managed entirely in software; no hardware tablewalks are performed. A TLB miss generates a fault, which the system software can handle as needed. A software-managed MMU is necessarily slower than one with an automatic hardware replacement mechanism. On the other hand, such designs allow more freedom and flexibility for the designer, who can determine the replacement policy or lock entries in the TLB.

IBM added a small four-entry micro-TLB on the instruction side to enhance the 403GC's performance. This technique was also used in the 601 to avoid contention between code fetches and load/store operations. If a code reference misses the micro-TLB, it is fetched from the main TLB with only a two-cycle penalty. Unlike the main TLB, the micro-TLB is managed entirely by hardware and is generally invisible to the programmer.

New Chips Give Designers New Choices

Not surprisingly, all three chips deliver nearly identical integer performance as a function of clock rate. On the wobbly foundation of Dhrystones/dollar, all three are bargains, offering performance similar to a 29040 or 960CF at a better price. The two 52-MIPS Motorola parts are within range of a 62-MIPS 960CF at the same clock speed. But at more than $120, the Intel part is almost twice as expensive and has almost no peripherals. Conversely, a similarly priced 960CF-25 puts out about 33 Dhrystone MIPS, one-third less than the PowerPC processors. The 5-V 960CF also draws 5 watts (typical)—an order of magnitude over the 3.3-V Motorola devices and

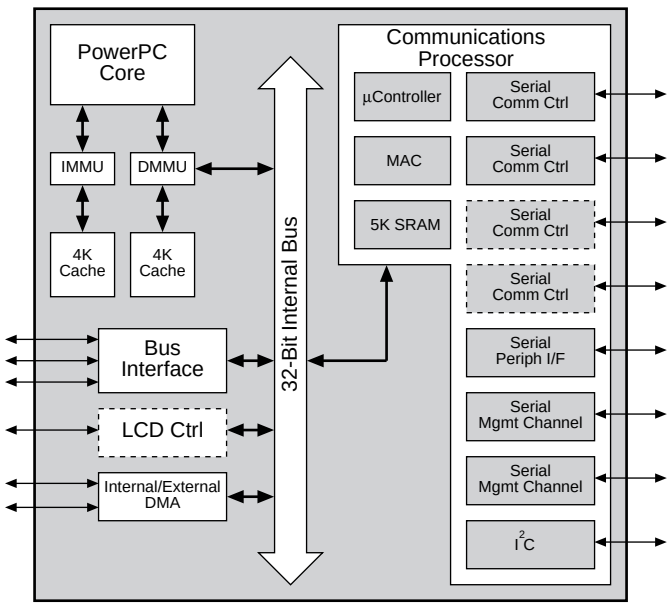

Figure 1. Block diagram of the 821 and 860 shows the similarities between the two devices. Except for the 821's LCD controller and the 860's two additional serial channels, the two are identical.

16 times what IBM's 403GC typically draws.

Motorola's edge in peripheral integration is evident here with the 821 and the 860. The company has repeatedly and successfully merged its microprocessor and data-communications designs to produce attractive, well-targeted devices. The 860 offers a big performance upgrade to users of the 68360 who need more application horsepower. The 821, like all PDA processors, will be a tougher sell. Motorola has lined up support for real-time operating systems like VxWorks, C Executive, Nucleus, and OS-9 from Microware (of which Motorola now owns 11%, with an option for another 13%). Established PDA operating systems such as Magic Cap or Newton are conspicuously absent. Without one of these PDA design wins, Motorola will have to find a customer that can make its own way in the PDA marketplace—like itself.

The company certainly has the wherewithal to fund a port of either Newton or Magic Cap to the 821 and then build and sell the devices through its wireless data communications division. Motorola already has a license for Newton. But with StrongARM processors on the horizon, Apple may be less eager than was once reported about migrating Newton to PowerPC; that task may fall to Motorola. Magic Cap is another alternative; Motorola already produces a 68349-based Envoy. However, General Magic is rumored to be busy moving Magic Cap to MIPS and may not have time for yet another port.

New Variations on the Horizon

With the 821 and 860, Motorola is now following the same strategy it did with the 68300 family, but with more performance. With 68K cores at the low end, ColdFire *(see **091203.PDF**)* in the middle, and PowerPC at the top, the possibilities for customization are many and varied.

IBM has been fast out of the gate, but its parts are hard to differentiate. Users who want a low-cost plain-vanilla PowerPC chip, though, now have the option of picking up an MMU.

IBM's strategy with the 400-series devices is to let its new customers define the products. Given the embedded PowerPC division's short time in existence, and with only one core and a limited peripheral library to work with, it is not surprising that the first three chips are so similar. As the company builds its selection of cores at the high and low ends and converts its own in-house peripheral blocks, IBM should be able to move the product line outward into other markets. When that happens, IBM should have more market flexibility than Motorola, which must restrict its embedded PowerPC line to the high end or risk attacking its own ColdFire and 68300 families.

We except PowerPC to become a popular embedded processor over the coming years, in part because of its "brand name" recognition and broad, expanding software support. These six chips promise to be just the beginning of a large and long-lived family. ♦

