Most Significant Bits

Cyrix Spills Performance Data on 5x86, M1

With its first release of performance data for its 5x86 processor, Cyrix has confirmed the old saw: you can prove anything with statistics. Depending on which benchmark you choose, a 100-MHz 5x86 is either significantly slower than, exactly the same as, or much better than a 75-MHz Pentium. The table below shows results for two key benchmarks, as provided by Cyrix.

System	Processor	Winstone95	CPUmark16
ECS UM8810 PCI	5x86-100	127.1	132.7
Chicony 471A	5x86-100	117.3	128.8
Dell XPS 75	Pentium-75	116.9	156.4
Gateway P5-75	Pentium-75	124.1	157.6
Micron PowerStation	Pentium-75	124.2	158.9
Cyrix average	5x86-100	122.2	130.7
Intel average	Pentium-75	121.7	157.6
Cyrix advantage		+0.4%	–17%

According to Winstone95, a system-level benchmark run under Windows for Workgroups 3.11, the average score of the two 5x86-based systems is nearly identical to the average score of the three Pentium boxes, with a difference of less than 1%. On CPUmark16, however, the 100-MHz 5x86 is about 17% lower than the 75-MHz Pentium, making it the equivalent of a 62-MHz Pentium. Cyrix also provided results for "toy" benchmarks, such as PowerMeter and Norton, that fit entirely in the on-chip cache; on these tests, the 5x86 outruns the Pentium by up to 11%. These last two tests, however, do not correlate well with real applications.

Winstone provides the best representation of application performance among these benchmarks, and the scores give validity to Cyrix's claims of matching Pentium-75 performance. CPUmark is a synthetic benchmark that, despite its name, includes a large number of main-memory accesses; the 5x86 suffers on this test due to its 32-bit 486-style bus that provides less than half the bandwidth of Pentium's bus. The 5x86's performance will diminish for programs that access memory more than those in the Winstone suite.

Cyrix also provided the first actual performance data on its flagship M1 processor in an attempt to claim performance leadership on Windows 95. Using an off-the-shelf Micron Millenia system, Cyrix measured a 100-MHz M1 at 164 running the Winstone95 benchmark under Windows 95; in the same system, a 133-MHz Pentium scored 3% less, according to Cyrix. The high-end system configuration included 256K of synchronous cache, 32M of EDO DRAM, and the Triton chip set, which is not optimized for Cyrix processors.

Cyrix further claimed to be faster than Intel's forthcoming P6 processor, based on Intel's own estimates that a 150-MHz P6 will be slower than a 133-MHz Pentium on 16-bit applications like the ones used in Winstone95 *(see **091001.PDF**)*. Intel projects that P6 performance will increase by 50% on the 32-bit applications that will typically be used with Windows 95; it is doubtful that the M1 will increase as much.

Intel responded to Cyrix's claim by reporting a 175 Winstone95 score using Windows 95 on a Triton-based motherboard with 256K of synchronous cache and 16M of EDO DRAM. Winstone scores are highly dependent on graphics and disk subsystems, however, making it difficult to use this metric to compare CPU performance. Cyrix also ran CPUmark16 on the M1 in the Micron system, reporting a score of 270, versus 258 for a 120-MHz Pentium. Cyrix reported no score for a Pentium-133.

Whether or not the M1 is faster than the fastest Pentium, Cyrix's initial test results should help it position the 100-MHz M1 against 120- or even 133-MHz Pentiums, satisfying the company's goal. For the first time, Cyrix will be able to match Intel's performance to the top of its line—at least on 16-bit applications.

AMD Preparing X5

Taking a page from Cyrix's marketing handbook, AMD confirmed it is developing an x86 processor that will be marketed as the X5. The company said the X5 will fit in performance between its current 486 line and the forthcoming K5 but will not use the K5 core. AMD would not offer further details on the unannounced product, but sources indicate that the X5 will use AMD's existing 486 core, combined with a 16K write-back cache.

In fact, the X5 may simply be a faster version of AMD's 486DX4, which currently runs at 120 MHz in a 0.5-micron process; the company previously said that it will move the 486 to its new 0.35-micron process, boosting the clock speed to 133 MHz and possibly beyond. Such a part would easily match the integer performance of entry-level Pentium processors while maintaining the low cost structure of a 486 system.

The X5 moniker contains the magical number that allows AMD to position its new product as a 586-class device, just as Cyrix is now doing with its 5x86. With the 486 rapidly going the way of the carrier pigeon, a new name could boost sales—if buyers accept it.

Intel Sneaks Write-Back into DX4

In an uncharacteristically low-profile move, Intel has added write-back capability to its DX4 chips. The new Writeback Enhanced IntelDX4 processors can operate the internal level-one cache in either write-through or write-back modes. Intel had previously added this ability to its 486DX2 processors, but the DX4 had remained

write-through only. The new DX4s are sampling now, with production expected later this month. Intel plans to convert all DX4 production to the new design by early next year, even as it is phasing out that device. There is no price difference between the write-back DX4 and the older product.

The write-back design offers slightly better performance, particularly in systems without an L2 cache. As the DX4 has become a low-end PC processor, it is more often used in cacheless systems, motivating Intel to make this change. More important, Intel's competitors offer write-back capability on most of their 486 processors, forcing Intel to play catch-up in this area. This change shows that Intel is not ready to abandon the 486.

TI Announces Low-Cost MVP

Cutting the price of its high-performance DSP, Texas Instruments has announced a lower-cost version of its powerful MVP chip, the 320C80. The new 320C82 carries a price tag under $100, less than half the price of the 'C80. The smaller chip achieves a peak rate of 1.5 billion operations per second using a 50-MHz clock.

The original MVP contains four DSPs, each capable of executing three operations per cycle, plus a RISC processor, dubbed the master processor, for control functions *(see **080405.PDF**)*. A complex crossbar bus allows multiple concurrent transfers among these processors as well as a total of 50K of on-chip SRAM.

The new chip uses a similar structure but has only two DSPs plus the master processor. The on-chip SRAM for this chip totals 44K: each DSP has 4K of instruction cache and 12K of data memory, while the master processor has 4K of instruction cache and 8K of data memory. Thus, although there are fewer processors, some applications will benefit because each processor has more on-chip memory.

Applications that require frequent accesses to external memory, however, will be slowed by a new multiplexed memory interface. The new interface, along with the elimination of the built-in video controller, reduces the number of external signals, allowing the 'C82 to fit into a lower-cost 240-pin PQFP. The new chip is built in a 0.5-micron CMOS process instead of the 0.6-micron process used for the 'C80, shrinking the die and further reducing cost.

Like its predecessor, the 'C82 can perform simultaneous H.320 encoding and decoding and thus is suitable for video-conferencing devices. It could also be used as a programmable accelerator in high-end PCs, providing MPEG-1 and MPEG-2 decoding, 3D graphics acceleration, and advanced audio capabilities. TI has not yet developed PC software for these functions, however, limiting the product's appeal in this market.

Vendors can now begin designing the 'C82 into their products, but samples will not be available until 2Q96, with volume production planned for 4Q96. In the meantime, designers can use the 'C80 as a development platform. At $82 in quantities of 25,000, the new part opens new markets for the high-performance DSP; even when the 'C82 finally reaches the market, the 'C80 will still be selling for about $250, according to TI. Most embedded products will make do with much less expensive DSPs, but for those products that need high performance, the 'C82 will fit the bill at a reasonable price.

Motorola Plans Move to 0.35-Micron

The recently unveiled 167-MHz PowerPC 603e *(see **0911MSB.PDF**)* will be built in a 0.35-micron CMOS process that IBM calls CMOS-5X *(see **090902.PDF**)*. IBM has been producing chips in this process since 4Q94, but Motorola has been struggling to reach the 0.5-micron level. Motorola now has the PowerPC 604 in production using a 0.5-micron process and plans a rapid jump to the next process level.

Using IBM's CMOS-5X to jumpstart its efforts, Motorola plans to bring its own 0.35-micron CMOS process on line by 1Q96, in time for volume production of the fast 603e parts. This quick move will bring Motorola's process technology more on par with that of the rest of the industry. The partners need to convert their entire PowerPC portfolio to the 0.35-micron level to stay competitive with Intel, which has been producing 0.35-micron Pentiums since 1Q95. The new 603e is the first step in this conversion.

Digital's Alpha Sales Growth Slows

For the first time in five years, Digital reported an annual profit: it earned $122 million in its fiscal 1995, which ended June 30. This profit is less than 1% of the company's total revenue of $13.8 billion but represents significant progress from previous results. Most of the improvement came on the cost side, as the company shed 21% of its workforce, or 16,000 people, during the year. Revenues were up just 3% from the previous year.

Digital did not provide specific breakdowns by product line, but a spokesperson said that Alpha products accounted for about $3 billion of the company's 1995 revenue, or nearly a quarter of the total. Assuming that Alpha systems have the same level of service revenue as Digital's other products, this works out to about $1.7 billion in Alpha hardware system sales, up from roughly $0.9 billion in 1994 *(see **0811ED.PDF**)*.

After several quarters of triple-digit annualized growth, Alpha sales increased only 32% in Digital's fiscal fourth quarter compared with the previous year, the company said. Alpha's initial growth came mainly from replacing VAX and MIPS machines in Digital's existing customer base. Now that transition is nearly complete, and new Alpha customers are harder to come by. Unless Digital can significantly expand the Alpha customer

base, sales of its RISC systems will reach perhaps $2.3 billion next year, less than 60% of Digital's combined VAX and MIPS system sales before Alpha's debut, and grow no faster than the overall market thereafter.

PA-8000 Gains Weight

At the recent Hot Chips conference, Hewlett-Packard revealed the transistor count and die size of its forthcoming PA-8000 processor *(see **081501.PDF**)*. The chip has 3.9 million transistors, which doesn't sound like much compared to a high-end processor like Digital's 21164, which weighs in at 9.3 million transistors, but the HP device has no on-chip cache. Thus, nearly all of its 3.9 million transistors are devoted to logic functions, making the PA-8000 CPU core almost twice as complex as any other announced RISC processor. Its nearest competitor, the R10000, uses 2.2 million logic transistors. The P6 CPU, with its CISC baggage, requires 4.5 million logic transistors, even more than the HP device.

Naturally, these transistors require quite a bit of silicon: the PA-8000 die measures 19.6 × 17.6 mm, or 345 mm^2, in a 0.5-micron four-layer-metal CMOS process. This makes the HP chip larger than any other modern RISC processor; at 314 mm^2, Sun's UltraSparc comes the closest. (Cyrix is currently building the M1 using a 394-mm^2 die but plans to shrink it later this year.) Combined with a package that we expect to have 700 or more pins, the PA-8000 will be more expensive to build than any of its contemporaries. HP hopes that the chip, due in systems in 1Q96, will make up for these deficiencies by outperforming all competitive processors.

Erratum: SGS-Thomson Resurrects Transputer

In our article on the SG20450 *(see **091003.PDF**)*, we reported, based on information from the vendor, that the chip uses a new CPU instruction set. In fact, the 20450 instruction set is nearly identical to that of SGS-Thomson's earlier RISC-like device, the Transputer. This similarity has helped SGS quickly gather a base of software and development tools for the "new" 20450.

The 20450 has some programming differences from the Transputer. Like the Transputer, the 20450 includes an on-chip microkernel implemented in microcode, but the newer device has a different system-level interface than its predecessor. Therefore, Transputer software written to use the microkernel will not run unchanged on the 20450. In addition, the newer chip features a different peripheral set and slightly modified serial links, so any Transputer code that uses these features must be changed. Otherwise, the programming model for the two chips is essentially the same. ♦

