Patent Watch

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently:

5,428,811
Interface between a register file which arbitrates between a number of single-cycle and multiple-cycle functional units
Issued: June 27, 1995
Inventors: Glenn J. Hinton, et al
Assignee: Intel
Filed: April 26, 1994
Claims: 13
A processor uses an interface protocol between a microprocessor register file and multiple first functional units which can independently execute first microinstructions that take multiple clock cycles to complete. The processor contains multiple second functional units that can independently execute second microinstructions that take a single clock cycle. The first and second microinstructions are issued by an instruction decoder. A microinstruction bus is connected to the instruction decoder, to the register file, and to each of the first and second functional units.

A line connects the instruction unit, the register file, and each of the first and second functional units, to signal that a current microinstruction on the microinstruction bus is valid. Hardware in the register file deasserts this line when any one register in the register file needed by the instruction on the microinstruction bus is busy. A write line connected from one of the single-cycle functional units to the multiple-cycle functional units is asserted by one of the single-cycle functional units upon the condition that the single-cycle functional unit requests access to the destination bus. Arbitration in each of the multiple-cycle functional units responds to various conditions to prevent access to the bus.

5,428,810
Allocation of resources of a pipelined processor by clock phase for parallel execution of dependent processes
Issued: June 27, 1995
Inventors: Anthony C. Barkans, et al
Assignee: Hewlett-Packard
Filed: March 31, 1994
Claims: 7
A technique of processing pipeline commands in parallel so as to minimize pipeline stalls. This is accomplished by arbitrating access to critical pipeline resources on the phase of the system clock. For example, one control process may access the critical pipeline resource only during an even phase of the system clock, while a second control process may access the critical pipeline resource only during the odd phase of the clock. These processes may run at the same time if the pipelined instructions being executed by each process have no data dependencies.

5,428,808
Single-chip microcomputer
Issued: June 27, 1995
Inventors: Terumi Sawase, et al
Assignee: Hitachi
Filed: March 25, 1994
Claims: 11
A logic circuit built in a single-chip microprocessor is built using electrically programmable memory elements, and information is written into the memory elements from outside, whereby a logic circuit having any desired logical functions can be constructed. The writing operation of the memory elements can be executed in a short time, and a user can obtain the single-chip microprocessor having hardware of particular specifications in a short period.

5,428,807
Method and apparatus for propagating exception conditions of a computer system
Issued: June 27, 1995
Inventors: Francis X. McKeen, et al
Assignee: Digital
Filed: June 17, 1993
Claims: 9
A mechanism for propagating exception conditions in a computer system when instructions are subject to exception conditions. The apparatus includes a set of data registers and a set of state registers for storing speculative states. There is one state register associated with each data register. The apparatus also includes a logic circuit, coupled to the set of state registers, for propagating the states from a source of one of the state registers to a destination one of the state registers, if data stored in an associated source of one of the data registers is used as a source for an associated destination of one of the data registers, and if data stored in the source data register is manipulated by a particular instruction subject to an exception condition.

Other Issued Patents
5,426,752 *Method for allocating real pages to virtual pages having different page sizes therefrom* ♦

