Patent Watch

by Rich Belgard, Contributing Editor

The following U.S. Patents related to microprocessors issued recently:

5,434,985
Simultaneous prediction of multiple branches for superscalar processing
Issued: July 18, 1995
Inventors: Philip G. Emma, et al
Assignee: IBM
Filed: August 11, 1992
Claims: 27
System and method for predicting a multiplicity of future branches simultaneously from an executing program, to enable the simultaneous fetching of multiple disjoint program segments. Additionally, the invention detects divergence of incorrect branch predictions and provides correction without penalty. By predicting an entire sequence of branches in parallel, the invention removes restrictions that decoding of multiple instructions in a superscalar environment must be limited to a single branch group. As a result, the speed of superscalar processors can be significantly increased.

5,432,918
Method and apparatus for ordering read and write operations using conflict bits in a write queue
Issued: July 11, 1995
Inventor: Rebecca L. Stamm
Assignee: Digital Equipment
Filed: June 22, 1992
Claims: 18
A method and apparatus for controlling memory access operations of a pipelined processor using a "write queue" are described. The write queue temporarily stores addresses of writes not yet made in memory. Each write-queue entry includes a write-read conflict bit. When an entry is first put into the write queue, the write-read conflict bit is cleared. When a subsequent memory read request occurs, the address of the read request is compared with the addresses stored in the write queue. If there is a match, the write-read conflict bit in the matching entry is set. If no conflict bits are set after this comparison, the read is allowed to proceed to memory before the queued writes. On the other hand, if any conflict bits are set, the read is prevented from proceeding. The write queue is able to accept additional entries while a read request is stalled.

5,430,888
Pipeline utilizing an integral cache for transferring data to and from a register
Issued: July 4, 1995
Inventors: Richard T. Witek, et al
Assignee: Digital Equipment
Filed: October 26, 1993
Claims: 2
A load/store pipeline in a computer processor for loading data to registers and storing data from registers has a cache memory within the pipeline for storing data. The pipeline includes buffers that support multiple outstanding read misses. Data from the pipeline is obtained independently of the operation of the pipeline corresponding to the misses. The cache memory can then be filled with the requested data.

5,430,851
Apparatus for simultaneously scheduling instruction from plural instruction streams into plural instruction execution units
Issued: July 4, 1995
Inventor: Hiroaki Hirata
Assignee: Matsushita
Filed: June 4, 1992
Claims: 46
An information processor comprising multiple instruction setup units that fetch and decode instructions as the first half of the procedure in instruction pipelines, each of the instruction setup units being in charge of processing instruction streams. The decoded results are scheduled in instruction schedule units and sent to each corresponding function unit to be executed.

Other Issued Patents

5,430,857 *Method and apparatus for translating logical addresses into physical addresses using odd/even translation tables*

5,430,856 *Data processing system simultaneously performing plural translations of virtual addresses having different page sizes* ♦

