Hitachi Adds FP, DSP Units to SuperH Chips

Two New Additions Aimed at Boosting Lead in Consumer Electronics

by Jim Turley

Seeking to cement its position as the highest-volume supplier of 32-bit RISC microprocessors, Hitachi is adding both floating-point and digital-signal-processing units to its successful SuperH product family. The new cores, dubbed SH-3E and SH-DSP, will form the basis for a series of new microprocessors.

Hitachi's Jim Slager, speaking at the Microprocessor Forum in October, said the first new chip, the SH7718, will use the SH-3E core to create a SuperH chip with an FPU that is pin-compatible with existing SH chips. The first SH-DSP chips are not expected until 2H96.

New Features Are Backward Compatible

One of the ingredients of Hitachi's current success in consumer electronics has been the SuperH core's fixed 16-bit instruction word. The stubby instructions keep code density very high but also lead to some awkward programming practices. For example, with only 12 bits available for an immediate offset, SH programmers must jump in 2K hops. The compact instruction encoding allows only two of the architecture's 16 registers to be accessed per instruction, necessitating destructive two-operand calculations.

Because there is little room for expansion in the already compact SH instruction set, Hitachi extended the instruction word to 32 bits for most new DSP-related instructions. The first four bits allow the instruction decoder to distinguish between existing SH instructions and, if the first four bits are all ones, a new 16-bit FP or 32-bit DSP instruction. In the case of a DSP instruction, the second 16-bit word is transferred to the DSP function unit while the first 16 bits control the integer unit. Table 1 lists the new FP instructions.

Mnemonic	Description
FMOV	Floating-point move
FLDI0	Load immediate zero
FLDI1	Load immediate one
FADD	Add
FSUB	Subtract
FMUL	Multiply
FDIV	Divide
FMAC	Multiply-accumulate
FCMP/EQ	Compare equal
FCMP/GT	Compare greater than
FTST/NAN	Test not-a-number
FNEG	Negate
FABS	Absolute value
FSQRT	Square root
FLOAT	Convert integer to float
FTRC	Truncate and convert to integer
FSTS	Store from system register
FLDS	Load to system register

Table 1. Hitachi's new SH-3E core design adds a number of basic floating-point functions to the compact SH instruction set.

SH-3E Extends Register, Instruction Sets

Both the SH-3E and SH-DSP cores are derived from Hitachi's third-generation core design, which is used in the SH7702 and SH7708 *(see **090302.PDF**)*. As such, the new chips share the same integer instruction set, including a 32-bit MAC. The 7718 will include the 7708's MMU, 8K unified cache, and assortment of timers and peripherals. The part will initially run at 66 MHz, though the company anticipates that a 100-MHz version will follow sometime in 2H96.

To accommodate single-precision floating-point values, the SH-3E core includes a set of additional registers. Sixteen 32-bit FP registers complement the standard set of integer registers.

The new FADD, FSUB, and FMUL instructions each execute with single-cycle throughput and a two-cycle latency. The FMAC instruction also has a single-cycle repeat rate, allowing $32 \times 32 + 32 \rightarrow 32$-bit operations. Floating-point division and square-root calculations complete in a respectable 13 cycles each.

Core Stays Small, Even with FPU

Hitachi is using an advanced 0.35-micron three-layer-metal process for the 7718. In that geometry, the

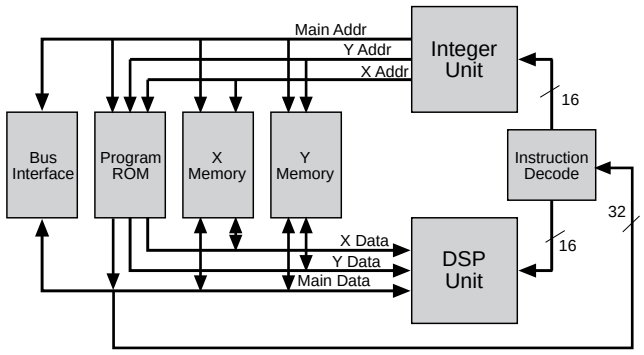

Figure 1. Hitachi's SH-DSP combines a DSP execution unit with the conventional SuperH integer core. The two execution units share internal buses and execute from a single instruction stream.

floating-point ALU, register file, and related logic double the size of the basic SH-3 core. But this increase represents less than 3 mm^2—a fair tradeoff for those applications that need to handle single-precision FP numbers without sacrificing software compatibility.

Also included are an on-chip DRAM controller, complete with two RAS, four CAS, and four WE signals, a half-dozen chip-select outputs, and four multiplexed interrupt inputs. Like most SH parts, the 7718 supports both big- and little-endian byte ordering.

DSP Adds Second Execution Unit

The SH-DSP represents a much more substantial extension of the SuperH core than any previous implementation. Hitachi added a separate DSP execution unit and restructured the on-chip cache and buses.

The DSP execution unit includes its own ALU, a barrel shifter, and a 16-bit multiplier that can perform $16 \times 16 + 32 \rightarrow 40$-bit operations with single-cycle throughput. The DSP also includes its own register file, with six 32-bit registers and two 40-bit accumulators. These additional registers are visible only to the DSP unit and to DSP-extended load/store instructions.

The DSP unit adds a fairly rich set of new functions, including modulo addressing capability, zero-overhead loop control, and indexed addressing with automatic pointer updating. In the best case, the SH-DSP can execute one ALU operation, one multiply, and two load/store operations at once.

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Jim Slager explains the features of Hitachi's SH-3E and SH-DSP at the Microprocessor Forum.

All DSP instructions are decoded and dispatched to both the conventional integer unit and to the DSP unit. The two units do not execute instructions in parallel, because they share the chip's internal address and data buses. Rather, the integer unit assists the DSP unit by generating addresses and executing load/store operations.

The 8K cache has been replaced by X and Y data memories, each 4K in size. Separate X and Y addresses driven by the integer unit are routed to both of these data memories and to an on-chip ROM, as Figure 1 shows. Likewise, X and Y data buses route data or ROM-resident constants to the DSP unit. This "extended Harvard" architecture is typical of DSP chips. In conjunction with the conventional on-chip address and data buses, the SH-DSP is able to access two data operands and fetch an instruction during a single cycle.

According to Hitachi's own simulations, a 60-MHz SH-DSP stacks up well against existing conventional DSP chips, with performance comparable to the TI C54x, AT&T's DSP16xx chips, and the Analog Devices 21xx family, all of which run at a slower clock rate.

Price & Availability

The first processor based on the SH-3E core, the SH7718, will begin sampling at 66 MHz in 1Q96, with production scheduled for 3Q96. General sampling of the first SH-DSP chip will begin near the end of 1996. Pricing has not been disclosed. For more information, call Hitachi America (Brisbane, Calif.) at 800.285.1601, extension 27.

FP, DSP Important Levers

Hitachi is not the first vendor to mix an integer unit with a DSP. Motorola's 68356, for example, merges a 68000 CPU with the company's 56002 24-bit fixed-point DSP unit. The result is similar to the SH-DSP—a single chip that contains two very different execution units.

In Motorola's case, however, the two execution units are more independent than they are on the SH-DSP. The 68K core executes its own code in parallel with DSP operations. The two instruction streams are kept separate by having individual address and data buses on the 68356 for the two cores. The Hitachi chip, on the other hand, executes a single instruction stream.

Hitachi's approach is an interesting one, and so far unique in the microprocessor world. It has become routine for 32-bit CPUs to include an independent on-chip floating-point unit or even additional integer ALUs, but the SH-DSP is the only one to include a DSP unit and treat it as part of the basic core.

Hitachi's two designs—the 3E and the DSP—are aimed at different markets. By adding single-precision floating-point to the 3E, Hitachi is hoping to penetrate further into the "consumer 3D" market for video games and set-top boxes. The SH-DSP, on the other hand, should help the company in multimedia and wireless communications applications.

Historically, Hitachi has undertaken significant CPU development at the behest of a customer with a large volume potential. The company has not yet identified which customers are waiting in the wings for the 3E and the DSP, in deference to those companies' wishes.

Hitachi has shown it can successfully deliver chips for high-volume, low-cost consumer designs. If the company can dispense basic FP and DSP functions as successfully as it has basic integer CPUs, it is likely to become an even bigger force in the under-$200 consumer marketplace. ♦

