Pentium Pro Debuts with Few Bugs

Initial Errata Sheet Shows Only Minor Problems

by Linley Gwennap

Living up to its promise, Intel has rolled out an errata list for its 150-MHz Pentium Pro processor within days of the product's formal introduction *(see **091501.PDF**)*. The microprocessor leader also continues to publish monthly updates of its Pentium errata list *(see **090303.PDF**)*, ensuring that all system designers, software developers, and end users have access to known bugs and other problems. Unfortunately, Intel's major competitors continue to hide their problems (see sidebar), much to the frustration of some users.

Although the Pentium Pro (PPro) errata list contains 30 problems, 10 have been fixed in the current C0 stepping, as Table 1 shows. (The B0 stepping was used for engineering samples and some early shipments.) Nine of the bugs in the C-step are expected to be fixed in the next stepping, while the remainder have simple workarounds and so are deemed "features" to be documented instead of repaired. Most of the nine bugs to be fixed occur only when the chip is in unusual modes that end users are unlikely to encounter.

Intel has not released the errata list for the 0.35-micron Pentium Pro processors, which operate at speeds up to 200 MHz. The company says that these processors have a subset of the errata listed in Table 1; a complete disclosure is due by the end of December. All 0.35-micron parts to date use the sA0 stepping, as Table 2 shows.

C-Step Looks Good; B-Step Is Rocky

The worst of the outstanding C-step bugs is number 20, which has the possibility of corrupting data in the system and thus could affect end users. The odds of encountering this problem are small. It occurs only if a

No.	Status	Errata (Description)
1	No fix planned	Mixed cachability of lock variables is problematic in MP systems.
2	No fix planned	FEA incorrectly calculated after FP access that wraps 64K boundary in 16-bit code.
3	No fix planned	Incompatibilities exist in debug exception reporting.
4	No fix planned	FLUSH# servicing delayed while waiting for SIPI in MP systems.
5	Fixed in C0	Fast-string-mode REP MOVS may not transfer all data.
6	Fixed in C0	Page-table base change during task switch using Mode C paging may corrupt EIP.
7	No fix planned	Code fetch that matches debug register may cause exception even if register is disabled.
8	No fix planned	Mode C paging in SMM causes use of incorrect page tables.
9	Fixed in C0	Memory indirect near call may corrupt EIP.
10	Fix planned	Single-bit correctable error in L2 cache may cancel simultaneous valid data.
11	Fixed in C0	Access across page boundary before write to CR3 may cause hang.
12	Fixed in C0	A20M# active during SMM dump.
13	Fixed in C0	Access across 4K-page boundary may cause hang.
14	No fix planned	Checker BIST failure in FRC mode not signaled.
15	Fix planned	BINIT# assertion causes FRCERR assertion in FRC mode.
16	Fix planned	Extra page fault may occur on IRET during task switch.
17	Fixed in C0	Some caching models in SMM may cause shutdown.
18	Fixed in C0	Fast-string mode reenabled after INIT event.
19	Fixed in C0	THERMTRIP# feature not present.
20	Fix planned	OUT instruction, branch trace message may write incorrect data.
21	Fix planned	THERMTRIP# pin not asserted for catastrophic thermal condition.
22	Fix planned	Last-branch-record (LBR) data may be written to last branch exception record (LBER).
23	No fix planned	Branch trace message (BTM) for SMI will contain incorrect FROM EIP value.
24	No fix planned	Task-switch fault may allow read access of linear address 00000000.
25	Fixed in C0	Low frequencies with 5/2 core-to-bus-clock ratio may fail in FRC.
26	Fix planned	Performance counters cannot be used in conjunction with SMM.
27	Fix planned	PWRGOOD forced low during boundary scan resets test access port (TAP).
28	Fix planned	BIST failure not indicated when RUNBIST TAP command is used.
1AP	No fix planned	APIC access to cachable memory causes shutdown.
2AP	No fix planned	MP systems may hang due to catastrophic errors during BSP determination.

Table 1. All published errata for Intel's 0.5-micron Pentium Pro processor, as of November 1995. AP indicates APIC (multiprocessor systems only). There are no current specification changes, as defined by Intel, for the Pentium Pro.

Processor Stepping	CPU_ID Family	Model	Step	Lot Numbers (on package)
P54C B1	5	2	1	SX874–910
P54C B3	5	2	2	SX921–51, SX960, SZ951
P54C B5	5	2	4	SX957–59, SX961–62, SX975, SZ977–SZ978
P54C C2 or mA1	5	2	5	SX963–70, SX994–98, SZ994–996, SU031–33, SK079–98
P54CS cB1 or mcB1	5	2	B	SU038, SK106–118
P6 B0	6	1	1	SY002, SY011, SY014
P6 C0	6	1	2	SY010
P6S sA0	6	1	6	SY012, SY013, SY024

Table 2. The stepping of a Pentium (P54C) or Pentium Pro (P6) processor can be identified via software, using the CPU_ID instruction, or by examining the lot number on the package. See text for description of steppings. Lot numbers for processors manufactured after 11/95 may not appear in this table.

data cache load that crosses a cache-line boundary is speculatively issued at the same that an OUT instruction or branch trace message (BTM) is dispatched. In some cases, the buffer that contains the data for the OUT or BTM is corrupted.

BTMs carry only debugging information, but OUT instructions send data to I/O devices. Thus, this bug could cause incorrect data to be written to a disk, printer, or network interface. Intel has supplied a BIOS patch to its OEM customers that avoids this problem.

A second C-step bug that might affect end users is number 10. Unlike most processors, PPro implements single-bit error correction for the L2 cache. Unfortunately, in some cases, the error correction fails, hanging the processor.

The other Pentium Pro bugs are fairly benign. Number 16 causes the page-fault handler to occasionally execute twice instead of once, causing an imperceptible performance loss but no data corruption. Number 15 occurs only in FRC (master-checker) mode, a mode used only in fault-tolerant designs and one that Intel has never gotten to work well in Pentium.

Numbers 22 and 26 affect only debugging software, while 27 and 28 affect only manufacturing tests. Number 21 prevents the THERMTRIP pin from signaling a thermal problem to external hardware; the processor still shuts down under extreme heat. An external thermal sensor can resolve this problem, if necessary.

Several of the B-step bugs can cause data corruption or system hangs and thus are visible to end users. Perhaps the worst is number 5, which describes situations in which the REP MOVS instruction fails to execute properly in "fast strings" mode, a problem exacerbated by number 18, which causes fast strings mode to be automatically reenabled after initialization. (The latter can be fixed with a BIOS patch.) But these and other critical problems are fixed in the C-step, which recently began production. We recommend avoiding the Pentium Pro B-step for revenue system shipments.

Cyrix, PowerPC Hide Bugs

Although several months have passed since Intel began publishing its bug lists, there has been little movement by other microprocessor vendors to match Intel's high standards. In particular, neither Cyrix nor the PowerPC vendors are willing to provide a public description of the bugs in their products, although both agree in principle that it is a good idea.

Cyrix argues that its small size prevents it from publishing bug lists in a timely fashion. (Its 5x86, for example, began shipping in August but still has no published errata list.) Cyrix hopes to publish 5x86 and 6x86 errata early next year but is making no promises.

Representatives from IBM and Motorola implicitly blame each other, claiming that the bureaucracy inherent in the partnership has prevented any progress on this issue. Of course, neither vendor publishes errata on the non-PowerPC processors that they produce independent of the partnership. The PowerPC 604 was riddled with bugs in its initial release, which delayed system announcements for several months *(see **090803.PDF**)*. The partners claim that these bugs have been fixed but are unwilling to document this claim.

AMD asserts that its 486 chips are bug-for-bug compatible with Intel's, as they share the same logic designs. The company promises to publish an errata list for the K5 when that product is shipping; delays in that program have given AMD a breather on this issue. NexGen has not published errata for its Nx586; once that company becomes part of AMD, it will presumably follow the parent company's guidelines.

Digital is one of the few companies to submit an errata list. According to the documentation, there are no outstanding functional errata for the 21064 or 21064A; the list contains only specification changes and clarifications.

Both MIPS Technologies, which was the first CPU vendor to publish errata, and Sun Technology Business (STB) publish errata lists for their processors on the Web. Errata for MIPS microprocessors can be found at *www.mips.com/htmls/mips_chip_rm.html;* for Sun chips, check *www.sun.com/sparc/microproc.html*.

Unfixed Pentium Bugs Accumulate

Intel appears overdue to release a new version of Pentium with fixes for several minor problems. Most of the parts built in 1995 have used the masks from the C2 stepping, which fixed the infamous FDIV bug (among other problems) but has since accumulated several outstanding problems. In fact, there are 22 errata that Intel plans to fix but are still present in current parts. The company expects new steppings that will fix most of these problems to begin shipping early next year.

Table 2 shows the various steppings for Pentium and lists the corresponding CPU_ID (used for software identification) and the lot numbers (inscribed on the

package). As implied by the CPU_ID, the mA1 stepping is logically identical to the C2 parts; the "m" indicates that these parts are Mobile Pentiums built to different voltage tolerances. The cB1 and mcB1 parts are also logically identical to the C2 stepping but are built on Intel's 0.35-micron process to achieve higher clock speeds.

Thus, all these parts have the same errata, except for those errata that affect unimplemented functions: the mobile processors do not implement the rarely used dual-processor (DP), FRC, or APIC functions. Some of the specification changes, such as voltage changes, affect only the mobile parts or the fast (cB1) parts.

No.	Status	Errata (Description)
24	Fixed in C2	FLUSH#, INIT, or machine check dropped due to floating-point exception.
25	Fix planned	Floating-point operations may clear alignment-check (AC) bit.
26	Fix planned	CMPXCHG8B across page boundary may cause invalid opcode exception.
27	Fixed in C2	Single-step debug exception breaks out of HALT.
28	Fixed in C2	Branch trace message corruption in slow-trace mode.
29	Fix planned	FRC lock-step failure during APIC write.
30	Fix planned	BE3#–BE0# sampled incorrectly at minimum Vih.
31	Fix planned	Incorrect PCHK# output during boundary scan in dual-processor (DP) mode.
32	Fix planned	EIP altered after specific FP operations followed by MOV Sreg, Reg.
33	No fix planned	WRMSR into illegal mode-specific register (MSR) does not generate GP fault.
34	Fixed in C2	Inconsistent data-cache state from concurrent snoop and memory write.
35	Fixed in C2	BE3#–BE0# not driven during boundary scan if RESET is high.
36	No fix planned	Incorrect value in floating-point instruction pointer (FIP) after RESET.
37	No fix planned	Second assertion of FLUSH# not ignored.
38	No fix planned	Segment-limit violation by FPU operand may corrupt FPU state.
39	No fix planned	FP exception inside SMM with pending NMI hangs system.
40	Fix planned	Supply current when in stop-clock state exceeds specification.
41	Fix planned	STPCLK# buffer samples incorrectly during boundary scan.
42	Fix planned	Incorrect decode of certain 0F-prefixed instructions.
43	No fix planned	Data breakpoint deviations.
44	No fix planned	Event-monitor counting discrepancies.
45	No fix planned	VERR-type instructions causing page-fault task switch with T-bit set may corrupt CS:EIP.
46	No fix planned	BUSCHK# interrupt has wrong priority.
47	Fix planned	BF and CPUTYP buffers sample incorrectly during boundary scan.
48	No fix planned	Matched but disabled data breakpoint can be lost by STPCLK# assertion.
49	No fix planned	STPCLK# ignored in SMM when INIT or NMI is pending.
50	No fix planned	STPCLK# pullup not engaged at RESET.
51	Fix planned	A fault causing a page fault can cause an instruction to be executed twice.
52	No fix planned	HLT when machine-check exception is pending can cause incorrect instruction or hang.
53	No fix planned	FBSTP stores BCD operand incorrectly if address wraps and FPU error occurs.
8DP	Fix planned	Incorrect assertion of PHITM# without PHIT#.
9DP	Fix planned	Double issuance of read cycles.
10DP	Fix planned	Line invalidation may occur on read or prefetch cycles.
11DP	No fix planned	EADS# or floating ADS# may cause extra invalidates.
12DP	Fix planned	HOLD and BOFF# during APIC cycle may cause dual-processor arbitration problem.
13DP	Fix planned	System may hang after hold during local APIC's second INTA cycle.
9AP	Fix planned	Spurious interrupt in APIC through-local mode.
10AP	Fixed in C2	Potential for lost interrupts while using APIC in through-local mode.
11AP	Fix planned	Back-to-back assertions of HOLD may cause lost APIC write cycle.
12AP	Fix planned	System hangs when BOFF# is asserted during second internal INTA cycle.
13AP	Fix planned	APIC pipeline cycle during cache-line fill causes restarted cycle to lose its attributes.
14AP	No fix planned	INIT and SMI via the APIC three-wire bus may be lost.
No.	**Status**	**Specification Changes (Description)**
12	Documented	STI (set interrupt flag) followed by FP instruction doesn't delay interrupt window.
13	Documented	IDT limit violation causes GP fault (should cause interrupt 8).
14	Documented	Dual-processor mode not supported in FRC systems.
15	mcB1 only	Decreased maximum power specification for mcB1 parts.

Table 3. All published errata and specification changes for Intel's P54C Pentium from March through November 1995. DP indicates dual-processor mode only; AP indicates APIC (multiprocessor systems only).

Remaining Pentium Bugs Are Obscure

As Table 3 shows, a large number of Pentium errata have been reported in the past several months. This number is probably indicative of the wide variety and immense amount of application software that runs on x86 processors rather than poor design on Intel's part. Most have been found by Intel's own testing rather than by end users. These bugs are all quite minor in most circumstances, and only a handful can affect end users.

Among the latter group are some that can cause data corruption in very obscure situations. Number 32 requires a specific sequence of FP instructions followed by a MOV from a segment register that misses the on-chip segment cache. Number 36 affects code that does not perform an FINIT after reset, as recommended. Number 42 occurs only when certain two-byte patterns occur exactly 33 bytes apart in certain instruction-cache locations. Number 53 involves the FBSTP (store BCD) instruction with unaligned operands.

Number 26 could crash programs that place the CMPXCHG8B instruction across a page boundary. This instruction is new in Pentium, however, so this bug cannot affect older code; most Pentium compilers are aware of this bug and ensure that this instruction is properly aligned. Similarly, number 38 can cause Pentium software to crash if there is a segment-limit violation during an FP store instruction, but this bug does not affect older code because the 486 and previous processors always crash in this situation.

Numbers 51 and 52 can cause data corruption, but neither can occur under any operating system that Intel has encountered. Number 51 is caused by a single instruction generating two specific faults before the OS can intervene. Number 52 happens when a machine check occurs while the processor is in a HALT state.

A plethora of problems (25, 43, 44, 45, 46, and 48) affect various debugging features and thus will not impact end users. For example, under certain circumstances, data breakpoints, event counters, and the alignment-check bit may not function properly. Numbers 31, 41, and 47 affect boundary-scan testing, typically performed during manufacturing only. Numbers 30, 37, 39, 40, and 50 have simple hardware workarounds. Other bugs affect only dual-processor (DP), fault-tolerant (FRC), or APIC-based multiprocessor (AP) systems.

Not As Bad As It Looks

Although the number of reported errata for Pentium is large, it is highly unlikely that an end user would encounter any of these problems. Intel works with most compiler, operating-system, and system-hardware vendors to ensure that the proper workarounds are in place. Even if the workarounds are omitted, the odds of these bugs occurring are tiny, even compared with the FDIV bug. Software developers encountering unusual crashes may wish to obtain a copy of Intel's errata documentation (see sidebar above) to check if their particular application is at higher risk than most.

As few other vendors have published errata sheets, it is difficult to compare the state of Pentium with that of other microprocessors. The MIPS R4400SC (revision 3.0) has 16 published errata, but that chip does not implement any multiprocessor functions; the MC (multiprocessor) version has 22 bugs. Some of the R4400 bugs appear more severe than Pentium's, however.

For example, one out of 22,000 randomly located jumps (J or JAL) will branch to the wrong destination, due to their instruction offset. This bug has a compiler workaround, but older code may be affected. Also, certain features in the chip, such as sub-block ordering and reduced power mode, simply don't work. The latter bugs, however, will not be visible to end users.

Digital claims to have no functional bugs in its 21064 and 21064A processors. This is an impressive achievement, undoubtedly aided by the relatively limited number of chip sets, system vendors, and applications that use the Alpha platform. Also, the company has not subjected its chip to the same rigorous testing as Pentium; Digital is more likely to have hidden bugs remaining in its processors.

Intel has made a major commitment to identifying and ultimately repairing defects in its chips. More than two years after the first Pentium processor was introduced, the company continues an extensive testing program aimed at discovering problems, which are then documented in the errata sheets. Most recent bugs have been found using random test code that is highly unlikely to be duplicated in real applications. Few, if any, other microprocessor vendors engage in this level of testing for products already in the field.

So far, Pentium Pro appears to be in good shape for a processor so early in its life cycle. Many PPro bugs were fixed before the chip was even released and probably would not have been published by other vendors. Intel has performed an unprecedented amount of testing on its new processor, both in-house and through the user community; as Pentium Pro becomes more widely used, we will see whether this testing succeeds in reducing the number of errata found in later revisions. ♦

For More Information

To receive a copy of the errata lists for the Pentium or Pentium Pro processors, contact Intel at P.O. Box 7641, Mt. Prospect, IL 60056 or call 800.879.4683; ask for the *Pentium* (or *Pentium Pro) Processor Specification Update*. For technical information on any of these errata, call Intel's support hot line at 800.628.8686.

