Most Significant Bits

Digital Speeds x86 Emulation

New emulation technology from Digital Semiconductor could give Alpha an edge in the Windows NT market. At Comdex, the company demonstrated an Alpha system running x86 applications at speeds of 70–90% of native Alpha code, according to the vendor. The new emulator, dubbed FX!32, is still under development, but Digital expects to release it as early as next spring.

The company did not disclose details of how it achieves such high performance but said that FX!32 is based on a combination of x86 translation and emulation rather than pure emulation. Digital has extensive experience with binary translation, delivering programs that translate VAX and MIPS binaries into Alpha code as part of the initial Alpha release.

By translating x86 instructions into RISC instructions (in this case, Alpha), the RISC processor executes the translated code at full speed without the awkward parsing and execution routines that slow standard emulators. In a sense, the translator is a compiler that starts with x86 binaries instead of high-level source code. Because pure binaries don't have the full information available from source code, the translator can't achieve the same performance as a true compiler, but theoretically, it can come close.

FX!32, as the name implies, is designed for programs that use the Win32 interface, that is, Windows 95 or NT applications. Operating-system calls from these programs are serviced by Windows NT running natively on Alpha, improving performance. Older code written to the Win16 model must be emulated by a product such as Insignia's emulator, which does not deliver the same level of performance as FX!32. As Windows 95 becomes the dominant PC operating system, most performance-sensitive applications should quickly move to Win32, supporting Digital's emulation strategy.

High-performance x86 emulation would help solve the lack of native business applications for the Alpha/NT platform. If FX!32 performs as claimed, a 21164 would offer Pentium-class performance when emulating x86 applications and Pentium Pro performance on native code, with superior floating-point speed. This combination would allow x86 users to move to an Alpha system without giving up their existing software. Digital's next problem will be to offer 21164-based systems at a price compelling enough to entice x86 users to switch.

Nx586 Gets FPU, Speed Boost

New chips from NexGen reduce the gap between Pentium and the Nx586 by adding floating-point capability and boosting the clock speed to match Intel's fastest parts. When NexGen first announced its Nx586 *(see **080403.PDF**)*, the company said it would offer the Nx587 as a math coprocessor for the FPU-less chip. The company has finally brought the 587 to market, but as an integral part of the 586 rather than a separate device.

Using IBM's multichip module (MCM) technology, NexGen has combined the 586 and 587 die in a single package. The new device, which uses the same pinout as its predecessor, is marketed as the Nx586-PF100 to distinguish it from the FPU-less Nx586-P100. The "P100" designation indicates NexGen's claim that the device offers performance similar to a 100-MHz Pentium; the NexGen chips actually cycle at 93 MHz.

Although there has been some dispute over NexGen's integer performance claims, the PF100 should compare well with Pentium on floating-point code. For basic operations, the NexGen part is actually faster, taking only two cycles for FP adds and multiplies, one cycle less than Pentium. Overall, the two chips should have similar FP performance.

NexGen also rolled out the long-awaited 0.5-micron version of its chips: the new P120 and P133 chips cycle at 120 and 133 MHz, respectively. Both new versions are currently sampling, and volume shipments are imminent. PF120 and PF133 versions (which include the floating-point unit) are due in 1Q96.

On CPUmark32, NexGen measured the 133-MHz Nx586, with 256K of asynchronous cache, at 248. Intel points out that a standard Pentium-133 system from Gateway, with 256K of synchronous cache, scores 278 on CPUmark32, 12% better than the Nx586. NexGen's design does not support the faster synchronous cache, but these figures indicate that a Pentium with a less expensive asynchronous cache would still outrun the Nx586, contradicting NexGen's claims that its processor is significantly faster than Pentium.

The new process provides a gate shrink only; the die size of the CPU remains 118 mm^2. The FPU die is a tiny 36 mm^2. The MDR Cost Model estimates the two-chip MCM costs $140 to build, 50% more than a Pentium-133. In quantities of 1,000, the PF100 is priced at $285, a $30 premium over the P100 version. By comparison, a Pentium-100 costs $300. NexGen's P120 and P133 list for $303 and $447, respectively, about 15% less than Pentium at the same clock speed.

Given that the NexGen part is not compatible with Pentium sockets and must use NexGen's PCI chip set, the 5% price saving offers little incentive for system makers to adopt the floating-point part. NexGen's FPU-less chips continue to offer a price advantage over Pentium and now span the key performance points. As demand for floating-point increases, however, NexGen will need to price its PF versions more aggressively.

PowerPC 603e, 604 Pick Up Speed

Moving to separate itself from Motorola, IBM is now shipping a 150-MHz version of the PowerPC 604 manufactured in its 0.35-micron CMOS-5X process. The company released some overinflated SPECint92 numbers in an unspecified system configuration. We project the chip will deliver 5.0 SPECint95 and 3.7 SPECfp95 (baseline) in a configuration similar to IBM's current 604-based workstations. This ranks the chip ahead of most shipping processors but behind Pentium Pro, Digital's 21164, and UltraSparc. The new 604, at $600, costs much less than these ultrafast processors.

Unlike previous IBM PowerPC announcements, this one was not matched by Motorola. That company is still struggling to build 120- and 133-MHz 604s on its 0.5-micron line while producing 100-MHz chips on its 0.65-micron process. Motorola is running test wafers on a new 0.35-micron fab and hopes to deliver products from this line, including faster 604s, in 1Q96.

Both companies announced a new speed grade of the PowerPC 603e: 120 MHz. This version uses a 0.5-micron process to achieve yield at that speed, although the die size stays the same. Motorola says it will begin shipping these parts by the end of the year; IBM has been shipping 117-MHz 603e chips to Apple for months and now will provide them to others.

IBM's $158 price for the 100-MHz 603e undercuts Motorola's $207 price, both in 1,000-unit quantities. This gap is typical of PowerPC pricing between the two vendors. But while Motorola is offering the 120-MHz version at $260, IBM is actually higher, at $309, perhaps to protect sales of its fastest 601 chips; Motorola, which doesn't build 601s, can be more aggressive.

Motorola's 100- and 120-MHz 603e prices are only slightly less than pricing for Intel's 90- and 100-MHz Pentiums, respectively. Based on SPECint92, the 603e delivers about the same integer performance as these Intel chips, albeit with significantly better FP scores. Intel's rapid price cuts *(see **0915MSB.PDF**)* have destroyed the PowerPC vendors' strategy of delivering similar integer performance for half the price.

IDT R4640 Lowers Cost of Orion

A new embedded MIPS processor in IDT's Orion line should appeal to cost-sensitive designers of midrange laser printers, datacom equipment, and high-end PC add-in products. The R4640 is a lower-cost alternative to the R4650 with a narrower data bus and a smaller package. Although the new 32-bit data bus reduces performance, it also cuts the chip's cost.

The internal core design of the 4640 is identical to that of the 4650 *(see **081504.PDF**)*, with a MIPS-III core that includes 64-bit registers and a combined integer/floating-point ALU. The 4640 exchanges its predecessor's external 64-bit multiplexed address/data bus for a narrower 32-bit bus, allowing the new part to fit into a smaller PQFP-128 package. Bus protocol and timing are unchanged. Apart from their buses, packages, and prices, the two chips are identical.

Like the 4650, the 4640 is available in 3.3-V and 5-V versions at three clock speeds. The company has begun sampling the 4640 at 80, 100, and 133 MHz, with production scheduled to begin in 2Q96. The two sibling CPUs are currently fabricated in the same 0.65-micron process, although IDT plans to shrink both to its 0.35-micron process in 1996, enabling faster 150- and 175-MHz versions of the parts later in the year. Eventually, the two chips will also share the same die.

The development of the 4640 is a tactical move that fills a hole in IDT's embedded processor lineup. Previously, there was a large price gap between the company's extended R30xx family and the R4650, the most affordable of its MIPS-III implementations. IDT has priced the 4640 about 40% less than the 4650; with 10K prices ranging from $28 for the 80-MHz version to $45 for the 133-MHz part, the 4640 creates an attractive bridge between the company's embedded MIPS lines.

From the Mailbox

If Apple truly meets its demise, it will be the largest public relations fiasco in computer history. It is not possible that Apple could have a more misguided PR and strategic advertising campaign. The entire program consists of highly defensive ads that tell current and prospective users *nothing* about the product's advantages. It is as if BMW devoted its entire ad campaign to criticizing Chevrolet.

Get rid of the market share foo-foo. The "10%" market share numbers are ridiculous. The computer market is highly segmented. Apple should identify itself as making "a better machine" and hammer, hammer, hammer that message. Maybe they could look at old Buick ads. ("Wouldn't you really rather own a Buick?") Or current BMW, Mercedes, or Lexus ads.

Then run killer ads showing that Apple has a better product on a feature-by-feature comparison. Apple should run ads showing learning time, mistake rates, etc., demonstrating with hard numbers that its systems are "engineered like no other computer" (or whatever slogan works). Right now, almost no one can rapidly name five things Macs still do better than Windows, yet there are probably thirty. (How about running really big programs, or upgradability, or support?) The vague perception is that Macs are better, but Apple doesn't offer a single tidbit to support that idea.

I am ready to write off Apple based on its own stupidity.

—Kim Rubin, VP Engineering,
GreenSpring Computers

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NEC Speeds R4300 to 133 MHz

NEC Electronics has begun sampling a 33% faster version of its R4300 processor. The new 133-MHz chip is reported to produce 80 SPECint92 and 60 SPECfp92, and it should deliver around 150–170 Dhrystone MIPS. The part will be priced at $35 in 100,000-unit quantities when it reaches production in 2Q96.

The R4300 was designed by MIPS Technologies specifically for NEC *(see **090601.PDF**)* and includes a 64-bit internal data path with a homogenized integer/FP execution unit. The design, which is based on the R4200 desktop processor, measures only 45 mm^2 in NEC's 0.35-micron process, including a 16K instruction cache, an 8K data cache, and a 32-entry TLB. While the chip is fairly low powered, with a 2.2-W typical power dissipation, it is not suitable for handheld applications. NEC is instead, like many other vendors, targeting set-top boxes, home and arcade video games, and multimedia products. The new version will not be used in Nintendo's Ultra 64, which relies on a 100-MHz R4300.

While the R4300's price/performance is impressive, it is not alone in that space. IDT's new R4640 (see previous item) is also stalking the same territory. Both are based on 64-bit MIPS-III cores with integrated FP units, dual caches, and 32-bit external buses. The chips are even offered at the same clock frequencies, and pricing is fairly similar; NEC's prices appear lower mainly because of its 100,000-unit lot size. The R4300's bus is easier to handle than the R4640's, but IDT has the advantage of core-logic chip-set support.

ARM Racks Up an Even Dozen

Advanced RISC Machines (ARM) has signed two additional licensees, bringing the total to 12 and making ARM by far the most widely licensed microprocessor architecture. The two new partners are Symbios (formerly part of NCR) and LG Semicon.

Symbios will use the ARM7 core in a new family of intelligent SCSI controller chips and other peripheral products. The company also licensed the Thumb code-compression module *(see **090401.PDF**)*. Symbios is a major player in the storage-controller chip market.

LG Semicon, seeking to extend its product line beyond DRAMs and other commodity parts, has licensed the ARM7 core (without Thumb) and the ARM710, a standalone microprocessor similar to the one used in Newton PDAs. LG plans to add the core module to its budding ASIC library in the hope of attracting designers of set-top boxes, PDAs, and multimedia enhancement products.

ARM's design team has been as busy as its marketing staff: the company announced a new integrated microprocessor, the 7100, for handheld devices. Code-named Eiger, the chip merges an ARM7 core, 16-level LCD controller, memory controller, MMU, 8K of cache, and several miscellaneous control functions. It runs at 18.4 MHz from a 32.768-kHz watch crystal, delivering about 15–18 Dhrystone MIPS. The 7100, which is expected to be used in Newton-based PDAs, will be fabricated by Cirrus Logic. That company expects to sell the 7100 for less than $25, with samples available in 2Q96.

New Tseng Chip Uses MoSys DRAM

The first standard product to take advantage of the revolutionary MoSys DRAM (MDRAM) is Tseng Labs' new ET6000, announced last month at Comdex. The new chip combines a fast 128-bit graphics accelerator, video acceleration features, clock generator, RAMDAC, and two MDRAM interfaces, creating a single-chip video subsystem with very high performance.

Tseng expects to sample the ET6000 by the end of the year, with volume production in 1Q96. In a 208-pin PQFP, the chip is priced at less than $30 in volume, which positions it against midrange DRAM-based graphics accelerators that offer significantly less performance.

For compatibility, the ET6000 also supports fast-page-mode and EDO DRAM, but MDRAM provides the best performance. At 50 MHz, the two MDRAM channels generate a peak bandwidth of 1.0 Gbytes/s *(see **081002.PDF**)*, improving the performance of the ET6000 compared with a standard VRAM design. Yet MoSys promises that its chips will carry little or no price premium over standard DRAM, making them much less expensive than VRAM for the same amount of frame buffer.

Further cost savings are achieved because MoSys's banked structure allows unusual memory sizes, such as 2.5M. This size matches the needs of a $1024 \times 768 \times 24$-bit display, whereas a standard DRAM or VRAM frame buffer must be 4M for this display.

The Tseng announcement is a big step forward for MoSys, helping the tiny memory vendor close the gap with Rambus, its key competitor. Although Rambus had a significant head start, only Cirrus offers a PC graphics controller that supports RDRAM *(see **0911MSB.PDF**)*. MoSys's deal with Tseng, just a few months behind the Cirrus announcement, puts the two vendors on nearly equal footing in the PC graphics area. Rambus still has an overall lead, however, with design wins at Nintendo, Chromatic, and Silicon Graphics.

MoSys also clarified its supply story. The fabless vendor will market MDRAMs built by IDT, Oki, and Taiwan's TSMC. None of these fabs will sell MDRAMs. As previously announced, SGS-Thomson plans to manufacture and market MDRAMs starting in mid-1996. MoSys is expected to announce its own MDRAM product plans by the end of the year. ♦

