MOST SIGNIFICANT BITS

Digital Regains Performance Lead

Achieving volume shipments of its 333-MHz 21164, Digital has announced immediate availability of the AlphaStation 600 5/333 with record-breaking SPECint95 performance of 8.34 and a SPECfp95 rating of 12.4 (base). The integer figure exceeds that of the 200-MHz Pentium Pro, which held the integer performance lead for about a month. (The 333-MHz Alpha chip had shipped in small quantities to a few Digital OEMs in December, but we did not count it as a volume product until now.) The 333-MHz AlphaStation carries a list price of $28,885 for a Windows NT-based version that includes a 4M external cache, 32M of memory, a 1G disk, CD-ROM, and a 17" monitor.

The company also announced a new AlphaServer with a 350-MHz 21164 processor but did not supply any SPEC95 ratings. This clock speed is achieved by handpicking the fastest parts from the 333-MHz bin; it will not be offered to external customers. Large numbers of 350-MHz chips will not be needed; the entry price for this top-of-the-line server is a stiff $319,000 for a two-processor system.

The announcements stave off attempts by SGI to claim performance leadership with its R10000 systems (see next item) and knock Intel out of the lead. But while the AlphaStation offers better price/performance than other high-end RISC machines, a 200-MHz Pentium Pro system from Intergraph delivers comparable integer performance, albeit lower floating-point, for less than $20,000. Users who don't need towering FP scores may be attracted to the Pentium Pro box, a trend that Digital must keep a watchful eye on.

R10000, R5000 Set for Extended Rollout

The formal announcement of the MIPS R10000 processor indicates that the chip, while nominally on schedule, will appear in systems slowly over the next several months. Both NEC and Toshiba announced that volume shipments will start as planned in March, and a few high-end servers should begin shipping at that time. Volumes will not be high enough to support workstation shipments until June.

Neither chip vendor appears eager to encourage customer orders. Toshiba has placed a $3,000 price tag (in volume) on the 200-MHz device, breaking the record for a single-chip microprocessor set by Digital's 21164, which began life at $2,937. NEC bluntly says "all early shipments are committed" and refuses to quote a price or a date at which it might take further orders. We believe the companies are still trying to get the large (298-mm^2) chip to yield in volume.

Silicon Graphics announced a slew of R10000-based systems, all using 200-MHz processors. Multiprocessor servers, mainly aimed at the supercomputer market, start at $88,800 and will ship in March. Indigo workstations featuring the new CPU start at $34,000 in a configuration with 1M of cache, 64M of memory, 2G of disk, and a 20" monitor.

These systems are measured at 8.11 SPECint95 and 10.5 SPECfp95 (base), slightly lower than the 333-MHz 21164. There is some headroom in these numbers: MIPS rates the 200-MHz R10000 at 9 SPECint95 and 19 SPECfp95 based on "future system designs and compilers that are currently being tested," a fancy phrase for vaporware. The huge increase in SPECfp95 will require a much larger L2 cache (4M–8M) and a faster memory subsystem, at minimum.

NEC also confirmed plans to ship a 275-MHz R10000 by 4Q96, using a 0.25-micron process shrink. This version is touted at 12 SPECint95 and 24 SPECfp95, putting it in *mano a mano* competition with future high-speed 21164 and UltraSparc-2 chips for the performance lead.

SGI also announced R5000 systems for March delivery, but with 23% lower performance than expected *(see* **100102.PDF***)*: the fastest system delivers just 4.0 SPECint95 and 3.7 SPECfp95 (base). Part of the gap is due to clock speed; although the chip was announced at 200 MHz, SGI reports it cannot purchase adequate quantities at that speed, so the initial systems are shipping at 150 and 180 MHz. MIPS believes that future compilers will eliminate the remaining performance gap. In the meantime, NEC expects to ramp production of 200-MHz R5000s in 2Q96.

Sun to Market Java Chips

Riding the wave of Java mania, Sun revealed plans to market a new line of microprocessors that will natively execute Java code. The line includes two devices, MicroJava and UltraJava, that will combine Java CPUs with unspecified system logic, such as a DRAM controller and peripheral bus interface. Sun Microelectronics (formerly STB) also plans to license the MicroJava CPU as an ASIC core under the name PicoJava. Sun expects MicroJava and PicoJava chips to sample in 1Q97, with UltraJava chips sampling late that year.

PicoJava and MicroJava are intended for embedded devices, such as cellular phones, PDAs, and video-game systems. Sun believes embedded designers will be attracted to Java because of its portability and ease of development. The more powerful UltraJava is designed for more general-purpose systems, such as the mythical Internet terminal and the "zero-administration client" that Sun's Scott McNealy has been promoting. Presumably, Sun will build UltraJava systems to extend the low end of its workstation line.

Java is an object-oriented programming language with syntax similar to C++. One feature of Java makes it particularly suited to Internet-based applications: instead of being compiled into binaries specific to a particular processor (e.g., SPARC or x86), Java applications are converted into a processor-independent byte stream. These Java bytes can then be executed on any processor running the Java virtual machine (VM). This feature allows the same Java code to run on any of a variety of host processors.

The drawback to this approach is that Java, like other interpreted languages, runs slowly: Sun estimates the performance gap between interpreted Java and optimized binaries is roughly 10×. Java can also be compiled, greatly improving performance, but this tactic leaves it no more portable than other programming languages. Dynamic compilation (performed on the host processor) improves performance while retaining portability, but at the cost of storing the compiler and its output locally.

The Java chips will improve performance without the overhead of dynamic compilation by directly interpreting and executing Java byte streams. Sun has not detailed this strategy but admits that some more complex Java instructions could be trapped and executed as a library call. Even executing some Java instructions natively should make these chips several times faster than similar non-Java processors interpreting Java code.

The success of the Java chips would then be tied to the usage of the Java language, which is small today but is expected by many observers to grow quickly. Sun hopes the performance of the new chips will be such that they can compete in embedded applications where Java is not used today, but the company has not released enough price or performance information to validate this positioning.

While Java is hot on the Internet, its appeal for embedded systems, most of which are not networked, is unclear. Most embedded designers would not want to give up 90% of their performance to switch to interpreted Java. For those who insist on Java, the PicoJava core may be interesting, but it must be backed by a complete ASIC program, which Sun does not offer. The company hopes to partner with one or more established ASIC vendors to solve this problem, but no such partners are yet announced. Thus, we expect the Java chips to find tough sledding in the embedded market. In networked computers, however, they could find a niche.

Intel Confirms 200-MHz Pentium Plan

As we speculated *(see* **1001MSB.PDF***)*, Intel will ship later this year a 200-MHz Pentium based on the current P54C design. The company confirmed that, although the P55C is expected to ship in 4Q96, these shipments will be too late for P55C systems to appear on shelves for the critical Christmas buying season. The 200-MHz device, expected to debut by midyear, will bridge this gap, providing a new high-end performance point for holiday shoppers.

The 200-MHz Pentium, however, may not deliver a significant performance boost over the current 166-MHz version on many applications. Although the core CPU speed is 20% higher, the bus clock remains at 66 MHz, and today's high-end Pentiums are frequently bottlenecked by bus bandwidth. Still, we expect the 200-MHz chip will sell well in the consumer market, where buyers tend to be less sophisticated.

More discerning business buyers are likely to avoid the Pentium-200. Fortunately, the business market is moving to Windows NT faster than previously expected. This move allows Intel to position Pentium Pro for high-end business buyers; the processor's problems with Windows 95 make it a poor match for the consumer market. To help accelerate Pentium Pro's adoption, Intel announced cuts of as much as 23% from its November prices, bringing the price of a 150-MHz PPro to $804. The 200-MHz version is now just over $1,000 *(see* **1002CW.PDF***)*.

Pentium prices plummeted, as usual, by 30% or more from the previous quarter. Even the fast parts announced just last month dropped by about 20%, putting the Pentium-166 at $620, about 20% below the slowest Pentium Pro. The biggest drop was for the Pentium-120 VRT, which fell 57%. It now carries a small premium over the standard 120-MHz Pentium; the slower VRT parts have no premium at all.

Intel is deemphasizing the 90-MHz Pentium, pricing it the same as the Pentium-100. The Pentium-75, reached a list price of $106 and is unlikely to go any lower; Intel seems to dislike two-digit prices. Instead, the price of the Pentium-90/100 will fall over time to the low-end price point.

The company expects the Pentium-120 to reach the low end by 4Q96. Its forecast includes a rapid phase-out of the 150-MHz Pentium Pro as prices of the faster versions decline. By year-end, 200-MHz PPro systems will sell for less than $2,500, according to the CPU vendor. This move will require PPro-200 prices to fall to about $500 by 4Q96, an aggressive pace that will put pressure on any Intel competitor that lacks a P6-class processor by that time.

Triton Gains USB, SDRAM Support

Improving on its already dominant Pentium chip set, Intel today announced two new versions of its 82430FX, better known as Triton. The 82430HX incorporates high reliability features for business PCs, whereas the 82430VX is tuned for multimedia performance and lower price points, appealing to the consumer market. Both new products offer several improvements over the existing Triton chip set.

That device processes one transaction at a time, stalling the PCI bus, for example, while an ISA transaction is in progress. The new chip sets allow concurrent operation on the CPU, PCI, and ISA buses, improving overall bus utilization. They also support delayed PCI transactions according to the PCI version 2.1 specification. Together, these features deliver better PCI bandwidth than any competitive chip set.

Intel also improved DRAM performance, achieving 6-2-2-2 reads at 66 MHz from EDO DRAM, one cycle faster than on Triton. The 430HX and VX are the first chip sets to include a USB port *(see* **090501.PDF***)*, which connects to emerging plug-and-play peripherals. Intel has promised to add this feature to all future chip sets.

The business chip set adds parity/ECC for the main memory, detecting and correcting errors. It supports up to 512M of DRAM, four times the capacity of Triton, making it suitable for low-end servers as well as desktop PCs. The HX consists of just two devices: a BGA-324 and a PQFP-208. This high-density packaging increases cost slightly but reduces

board space, giving designers flexibility to add features such as modems and videoconferencing to the motherboard. The HX is now in production at a 10,000-unit price of $37.50.

The VX consumer chip set does not support parity or large memory but adds synchronous DRAM support with 7-1-1-1 read access. Although SDRAM will slightly increase the performance of high-end boxes, most OEMs are likely to leave the cache out of SDRAM systems, lowering system cost but producing nearly the same performance as a 256K cache with standard DRAM. To further reduce the cost of low-end PCs, the VX also allows unified memory designs *(see* **090801.PDF***)*. Using the same four-chip configuration as Triton, this chip set lists for $33, a bit less than the HX.

As did Triton, these products set new standards for feature set and performance. In 1996, PC chip sets must offer USB and SDRAM support to be competitive. Intel claims that the improved DRAM timing and higher PCI bandwidth increase application performance by up to 10% compared with the original Triton, which already leads most competitors' chip sets in performance. This combination leaves Opti, SiS, and other chip-set vendors playing catch-up again.

First Alternative PPro Chip Set from VIA

Bringing the first competition to Intel's Pentium Pro chip set, VIA Technologies has launched its Apollo P6 chip set. The announcement shows there will be multiple vendors in the Pentium Pro chip set market, and it also exposes Intel's weaknesses; the Apollo product is superior to Intel's Orion in several respects.

While supporting systems with up to four processors, Apollo P6 consists of only three chips: the system controller (VT82C685), the data path (VT82C687), and the PCI-to-ISA bridge (VT82C586). In contrast, Orion requires eight chips to provide equivalent function. In addition to reducing the board space required, Apollo P6 puts fewer loads on Pentium Pro's GTL+ bus than does Orion. The VIA product integrates a USB interface, UMA support, SDRAM support, and enhanced IDE bus mastering; none of these features is provided by Intel.

The Apollo P6 chips are all in 208-pin PQFP packages and are built in 0.6-micron CMOS by Toshiba. Toshiba's participation is important for supplying the GTL+ I/O buffers needed to interface with the Pentium Pro bus. VIA's chip set also includes Intel's APIC circuitry, under license, to support multiprocessor systems.

Samples, expected in 1Q96, are priced at $89 per set; we project that volume pricing will be about $50 in 2Q96. In contrast, Intel sells Orion for $200–$300, depending on the configuration. Intel expects to launch a low-cost Pentium Pro chip set in 1H96 that should offer better competition to VIA's new offering.

These low-cost chip sets, combined with expected price cuts in Pentium Pro, should propel Intel's most powerful processors into mainstream PCs; by the end of this year, Pentium Pro systems should reach $2,500 price points. VIA appears to be in a good position to garner design wins, but it must demonstrate full compatibility with the complex Pentium Pro bus. The challenger must also come closer to Intel's performance than it has with its Pentium chip sets.

Exponential Tapes Out

Taking a major step forward, Exponential Technology today reported that it recently taped out its BiCMOS PowerPC processor *(see* **0917MSB.PDF***)* and expects to receive first silicon shortly. This puts the company on schedule to make first volume shipments in early 1997, as it had previously stated. The San Jose startup hopes the device will outrun all competitive microprocessors and fill the hole in the high end of the PowerPC lineup.

Exponential also signed licensing agreements with IBM and Motorola. The IBM agreement gives Exponential a full license to the PowerPC architecture and to "certain other patents" related to microprocessor design. The Motorola license covers IC manufacturing patents, avoiding any problems for Exponential's unnamed fab partner. Neither IBM nor Motorola gains any rights to build or sell the Exponential chip. The agreements should eliminate any potential legal issues with those two companies and allow the startup to freely market its processor.

ARM Proliferates to Oki

Worldwide support for ARM continues to build, as Oki Electronics has taken a license to the omnipresent architecture. Becoming the lucky thirteenth licensee, Oki now has access to the ARM7 core as well as the Thumb preprocessor *(see* **090401.PDF***)*. The Japanese semiconductor vendor plans to focus on application-specific chips for the auto-motive and peripheral markets, where the company has been successful with its 8-bit and 16-bit microcontrollers. Oki will also add the ARM7 core to its ASIC portfolio.

For the past three years, Oki has attempted to sell its own PA-RISC chips into the same markets. As we noted recently *(see* **091702.PDF***)*, these chips have not sold well, and the company has apparently decided to chart a new course. ARM has the advantage of multiple sources and a wide array of development tools, along with a clear growth path through the ARM8 and StrongArm *(see* **100201.PDF***)* cores. While Oki will continue to supply PA-RISC chips to its customers, it is likely to deemphasize that architecture in the future, instead pushing its ARM.

Errata: R5000 Cycle Times

Due to incorrect information from the vendor, the cycle times given in the previous issue *(see* **100102.PDF***)* for certain R5000 operations were too long. For integer multiplication, the R5000 has a throughput of three cycles for single precision and four for double precision; the latency is one additional cycle. For FP square root, the throughput is 19 cycles for single precision and 34 for double precision; the latency is two cycles longer. M

