PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments via e-mail to belgard@umunhum.stanford.edu.

5,461,718

System for sequential read of memory stream buffer detecting page-mode cycles availability, fetching data into a selected FIFO, and sending data without accessing memory
Issued: October 24, 1995
Inventors: David A. Tatosian, et al
Assignee: Digital
Filed: April 24, 1992
Claims: 18
A read-buffering system employs a bank of FIFOs to hold sequential read data for a number of data streams being fetched by a computer. The FIFOs are located in the memory controller. The buffer system stores read addresses from the CPU. If the CPU requests address N and N+1, a "stream" is said to have been detected, and data is fetched from DRAM memory for addresses following the requests. This prefetched data is stored in one of the FIFOs. If the CPU subsequently makes a read request for data that is in a FIFO, this data can be returned without making additional memory accesses. Page-mode access to DRAM can be transparent to the CPU.

5,457,802

Integrated-circuit pin-control apparatus and method thereof in a data-processing system
Issued: October 10, 1995
Inventors: Michael I. Catherwood, et al
Assignee: Motorola
Filed: May 17, 1993
Claims: 17
A data-processing system having address pins, data pins, control pins, chip-select pins, and other pins. For bus cycles of an instruction that do not require use of an external address bus, the values driven by the address pins are "frozen"in their previous logic state, that is, the most recent value driven by address pins during a bus cycle that required use of the external address bus. Data pins may be "frozen" in the same manner as address pins. Control pins, chip select pins, and other pins may be driven to their respective inactive logic states. The goal of the invention is to reduce noise and power consumption by reducing the voltage switching taking place on external buses and lines in the data-processing system.

5,457,790

Low-power-consumption semiconductor integrated-circuit device and microprocessor
Issued: October 10, 1995
Inventors: Masahiro Iwamura, et al
Assignee: Hitachi
Filed: October 18, 1993
Claims: 19
In a microprocessor including at least one function block, the start of the operation of the function block is detected prior to the start of the operation; the function block is activated prior to the start of the operation and inactivated after the termination of the operation.

5,455,955

Data processing system with device for arranging instructions
Issued: October 3, 1995
Inventors: Hiroyuki Kida, et al
Assignee: Hitachi
Filed: September 28, 1992
Claims: 24
The system translates an instruction word from main memory into an intermediate machine word having an orthogonal format, and addresses a microprogram memory corresponding to the instruction word by analyzing the intermediate machine word. The system further incorporates a plurality of register sets, so each different task can use an individual register set, and a memory for the number of registers holding global parameters used commonly among procedures corresponding to the register sets, so the number of registers for each can be changed arbitrarily.

5,455,924

Apparatus and method for partial execution blocking of instructions following a data cache miss
Issued: October 3, 1995
Inventors: Sunil R. Shenoy, et al
Assignee: Intel
Filed: February 9, 1993
Claims: 63
This data cache is partially blocking in that it will block the execution of any store instructions after an outstanding load instruction that missed the cache. The invention allows execution of subsequent load instructions while less than a predetermined number of preceding load instructions are still outstanding, as determined by a counter for outstanding load misses.

OTHER ISSUED PATENTS

5,463,748 *Instruction buffer for aligning instruction sets using boundary detection*
5,463,737 *Instruction buffer controller in processor enabling direct refetching of an instruction*
5,463,778 *User-controlled trap handler*
5,459,844 *Predecode instruction compounding* M