# Revised Model Reduces Cost Estimates 

## Pentium Manufacturing Cost Now Estimated at \$40, Pentium Pro at \$144

## by Linley Gwennap

We periodically refine the MDR Cost Model based on inputs from industry sources. This article presents the results of the latest revision. For more information about the Cost Model, refer to 081203.PDF and 071004.PDF.

As rapidly as microprocessor technology advances, the assumptions used to estimate manufacturing cost must also change. We recently revised the MDR Cost Model to more accurately project the cost of building high-end microprocessors. In general, these revisions have caused estimated costs to drop by $20-40 \%$.

The revised numbers emphasize that Intel's recent price cuts maintain a solid profit margin for the company, even at the low end. For example, a $75-\mathrm{MHz}$ Pentium today lists for $\$ 106$; we estimate its manufacturing cost is $\$ 49$. As the company moves most of its production to the 0.35 -micron level this year, costs will drop further: at this level, Pentium costs about $\$ 40$ to build, as Table 1 shows.

## Revisions to Wafer Cost, Test Time

The MDR Cost Model retains the same basic equations as in its original design (see 071004.PDF), but we have adjusted some of the input parameters. The most significant change is that wafer cost estimates have been adjusted downward. For example, we now estimate the wafer cost of Intel's 0.35micron four-layer-metal BiCMOS process at $\$ 2,700$, a $35 \%$ reduction.

The model includes in the wafer cost both the direct costs (labor and materials) to process the wafers and allo-
cated depreciation for the fab (clean room and equipment). The latter cost is increasing at a much faster rate than the former; for a 0.35 -micron process, depreciation accounts for about $60 \%$ of the wafer cost. The model assumes that fabs are running at or near full capacity; for vendors that cannot fill their fabs, the allocated depreciation becomes huge.

The equations used to calculate yield and die per wafer remain the same. An important factor in yield is defect rate. As a new process comes on line, its defect rate is high, but the rate drops as the process matures, a period that can last a year or more. We model this effect by reducing the defect rate over time from 1.0 defects $/ \mathrm{cm}^{2}$ for new processes to about 0.5 for mature processes. Thus, the cost estimate quoted for a processor in one quarter may be higher than the estimate provided in the next quarter. In particular, the figures presented here reflect the maturity of Intel's 0.35 -micron process, which has been in production for about a year.

Once the wafers are processed, the die must be tested to separate the good parts from the bad. The previous model, basing test time solely on transistor count, calculated that the 3.3-million-transistor Pentium would require four minutes of test time, driving test costs to $\$ 22$ per chip. The model has now been revised to account for the variety of techniquessuch as scan testing (e.g., JTAG) and built-in selftest (BIST) vendors use to reduce test time. Taking these factors into account, we now estimate the test time for Pentium (and similar chips) to be 30 seconds. This change reduces test cost significantly, to just $\$ 4$ in the case of Pentium.

The good die are then packaged for sale. The model now includes revised cost estimates for PGA packages that,

|  | Intel <br> Pentium | AMD <br> 5 K 86 | Cyrix <br> $6 \times 86$ | MIPS <br> R5000 | PowerPC <br> 603 e | PowerPC <br> 604 | Pentium <br> Pro | Sun <br> UltraSparc | Hitachi <br> SH7604 |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Type of process | BiCMOS | CMOS | CMOS | CMOS | CMOS | CMOS | BiCMOS | CMOS | CMOS |
| Process dimension (drawn) | $0.35 \mu \mathrm{~m}$ | $0.35 \mu \mathrm{~m}$ | $0.44 \mu \mathrm{~m}$ | $0.35 \mu \mathrm{~m}$ | $0.64 \mu \mathrm{~m}$ | $0.44 \mu \mathrm{~m}$ | $0.35 \mu \mathrm{~m}$ | $0.47 \mu \mathrm{~m}$ | $0.8 \mu \mathrm{~m}$ |
| Number of metal layers | 4 | 3 | 5 | 3 | 4 | 4 | 4 | 4 | 2 |
| Wafer size $(\mathrm{mm})$ | 200 mm | 200 mm | 200 mm | 200 mm | 200 mm | 200 mm | 200 mm | 200 mm | 150 mm |
| Estimated total wafer cost | $\$ 2,700$ | $\$ 2,200$ | $\$ 2,400$ | $\$ 2,600$ | $\$ 2,500$ | $\$ 2,300$ | $\$ 2,700$ | $\$ 2,200$ | $\$ 500$ |
| Die area $\left(\mathrm{mm}^{2}\right)$ | $91 \mathrm{~mm}^{2}$ | $181 \mathrm{~mm}^{2}$ | $204 \mathrm{~mm}^{2}$ | $84 \mathrm{~mm}^{2}$ | $98 \mathrm{~mm}^{2}$ | $196 \mathrm{~mm}^{2}$ | $196 \mathrm{~mm}^{2}$ | $315 \mathrm{~mm}^{2}$ | $82 \mathrm{~mm}^{2}$ |
| Effective area | $85 \%$ | $75 \%$ | $85 \%$ | $48 \%$ | $65 \%$ | $72 \%$ | $85 \%$ | $68 \%$ | $75 \%$ |
| Gross die per wafer | 297 | 159 | 122 | 325 | 275 | 128 | 128 | 74 | 177 |
| Estimated defects per $\mathrm{cm}^{2}$ | 0.6 | 0.8 | 0.7 | 0.8 | 0.5 | 0.8 | 0.6 | 0.8 | 0.5 |
| Yield percentage | $65 \%$ | $40 \%$ | $36 \%$ | $74 \%$ | $74 \%$ | $38 \%$ | $42 \%$ | $26 \%$ | $75 \%$ |
| Untested cost per good die | $\$ 14$ | $\$ 40$ | $\$ 55$ | $\$ 11$ | $\$ 9$ | $\$ 47$ | $\$ 50$ | $\$ 116$ | $\$ 4$ |
| Package size | 296 pin | 296 pin | 296 pin | 272 pin | 240 pin | 304 pin | 387 pin | 521 pin | 144 pin |
| Package type | PGA | PGA | PGA | PBGA | CQFP | CQFP | MCM | PGA | PQFP |
| Estimated package cost | $\$ 18$ | $\$ 21$ | $\$ 21$ | $\$ 11$ | $\$ 14$ | $\$ 21$ | $\$ 40$ | $\$ 45$ | $\$ 3$ |
| Total test $\&$ assembly cost | $\$ 8$ | $\$ 10$ | $\$ 10$ | $\$ 6$ | $\$ 6$ | $\$ 12$ | $\$ 21^{*}$ | $\$ 28$ | $\$ 1$ |
| Total manufacturing cost | $\$ 40$ | $\$ 71$ | $\$ 86$ | $\$ 28$ | $\$ 29$ | $\$ 80$ | $\$ 144 *$ | $\$ 189$ | $\$ 8$ |

Table 1. A detailed comparison of the manufacturing costs of several leading processors shows Pentium's significant cost advantage over its major $x 86$ competitors, although a few RISC chips deliver comparable performance at a lower cost. Pentium Pro's cost is less than that of any high-end RISC processor, including UltraSparc. *Pentium Pro cost includes 256 K cache chip. (Source: MDR Cost Model)
like Pentium's, use a staggered or interstitial array to reduce cost. The model also increases the volume discount that vendors such as Intel can obtain from package suppliers. We now estimate Intel pays $\$ 18$ for Pentium PGA packages.

These costs assume that a company is building a part in its own fabs and performing its own testing and packaging. A key exception to this rule is Cyrix, a fabless CPU vendor. For a product like the $6 \times 86$, the model's cost estimate reflects IBM's cost in producing the part; Cyrix purchases untested wafers from IBM and probably pays a small markup in this transaction. Companies that rely on their foundries to perform testing presumably pay a higher premium.

While fab depreciation is included in these costs, no account is made for allocated process development costs or CPU design costs. For example, Pentium is purported to have cost more than $\$ 100$ million to design, but this cost comes to less than $\$ 1$ per unit shipped. A low-volume processor like Alpha, in contrast, could carry hundreds of dollars per unit of amortized design costs.

## Intel Retains Cost Advantage

In the Pentium-class arena, the new estimates reinforce Intel's cost advantage. We now project the cost of AMD's 5 K86 to be $\$ 71$ and Cyrix's $6 \times 86$ at $\$ 86$, about twice the cost of Pentium. The primary difference is the die size of the parts: in a 0.5 micron process, Pentium is $27 \%$ smaller than the $6 \times 86$ while using one less metal layer. At the 0.35 -micron level, Pentium is $43 \%$ smaller than the 5 K 86 , although the Intel part requires one additional metal layer. Intel also gains a cost advantage over its competitors through sheer economies of scale, particularly in the packaging area.

Intel's competitors will gain slightly over time, as their parts are early in the learning curve and so have more room to fall in cost. Cyrix is already preparing to shrink the $6 \times 86$ to a $0.35-$ micron process, shaving $\$ 6$ off the cost. As both AMD and IBM (Cyrix's main fab) gain more experience at the $0.35-$ micron level, defect rates will fall and the costs of the 5 K 86 and $6 \times 86$ will drop to around $\$ 58$ and $\$ 64$, respectively. These costs will still be $50 \%$ larger than Intel's.

But when Intel deploys its forthcoming P55C Pentium, its manufacturing costs are likely to rise slightly due to the larger die of that chip. We estimate that the P55C's larger caches and other enhancements will increase the die size by $10-20 \%$. Because of the relatively small size of the current P54C design, however, the model calculates that this increase will add just \$2-\$4 to the total chip cost.

## Next-Generation Chips See Gains

The adjustment in costs had its biggest effect on the most advanced chips with the highest transistor counts. The cost estimates for next-generation RISC processors such as the MIPS R10000, UltraSparc-1, and the 0.5 -micron 21164 all dropped to about $\$ 200$ or below. At nearly $\$ 300$, HP's PA8000 remains the single-chip cost champion, due to its enormous die and generous (and still unspecified) pin count.

|  | Process | Die Area | Package | Est. Cost |
| :--- | :--- | ---: | :--- | :---: |
| R4700 | $0.60 \mu, 3 \mathrm{M}$ | $73 \mathrm{~mm}^{2}$ | MQUAD-208 | $\$ 23$ |
| MicroSparc | $0.80 \mu, 2 \mathrm{M}$ | $225 \mathrm{~mm}^{2}$ | TAB-288 | $\$ 26$ |
| PowerPC 603 | $0.64 \mu, 4 \mathrm{M}$ | $85 \mathrm{~mm}^{2}$ | CQFP-240 | $\$ 26$ |
| Cyrix 5x86 | $0.64 \mu, 3 \mathrm{M}$ | $144 \mathrm{~mm}^{2}$ | PGA-168 | $\$ 35$ |
| PowerPC 601+ | $0.33 \mu, 5.5 \mathrm{M}$ | $74 \mathrm{~mm}^{2}$ | CQFP-304 | $\$ 41$ |
| Pentium | $0.50 \mu, 4 \mathrm{M}$ | $148 \mathrm{~mm}^{2}$ | PGA-296 | $\$ 49$ |
| PowerPC 604 | $0.64 \mu, 4 \mathrm{M}$ | $196 \mathrm{~mm}^{2}$ | CQFP-304 | $\$ 57$ |
| PA-7150 | $0.80 \mu, 3 M$ | $196 \mathrm{~mm}^{2}$ | PGA-504 | $\$ 77$ |
| PA-7100LC | $0.80 \mu, 3 M$ | $196 \mathrm{~mm}^{2}$ | PGA-432 | $\$ 86$ |
| MicroSparc-2 | $0.50 \mu, 3 \mathrm{M}$ | $233 \mathrm{~mm}^{2}$ | PGA-321 | $\$ 92$ |
| 21064A | $0.50 \mu, 4.5 \mathrm{M}$ | $166 \mathrm{~mm}^{2}$ | PGA-431 | $\$ 98$ |
| PA-7300LC | $0.50 \mu, 4 \mathrm{M}$ | $259 \mathrm{~mm}^{2}$ | PGA-464 | $\$ 101$ |
| UltraSparc-2 | $0.29 \mu, 5 \mathrm{M}$ | $149 \mathrm{~mm}^{2}$ | PGA-521 | $\$ 108$ |
| HyperSparc* | $0.40 \mu, 3 \mathrm{M}$ | $135 \mathrm{~mm}^{2}$ | MCM-131 | $\$ 147$ |
| PA-7200 | $0.55 \mu, 3 \mathrm{M}$ | $210 \mathrm{~mm}^{2}$ | PGA-540 | $\$ 153$ |
| 21164 | $0.35 \mu, 4.5 \mathrm{M}$ | $209 \mathrm{~mm}^{2}$ | PGA-499 | $\$ 166$ |
| R10000 | $0.35 \mu, 4 \mathrm{M}$ | $298 \mathrm{~mm}^{2}$ | PGA-527 | $\$ 176$ |
| Pentium Pro* | $0.50 \mu, 4 \mathrm{M}$ | $306 \mathrm{~mm}^{2}$ | MCM-387 | $\$ 182$ |
| 21164 | $0.50 \mu, 4.5 \mathrm{M}$ | $310 \mathrm{~mm}^{2}$ | PGA-499 | $\$ 205$ |
| PowerPC 620 | $0.44 \mu, 4 \mathrm{M}$ | $311 \mathrm{~mm}^{2}$ | CBGA-625 | $\$ 211$ |
| PA-8000 | $0.50 \mu, 4 M$ | $345 \mathrm{~mm}^{2}$ | PGA-700? | $\$ 292$ |
| Power2* | $0.72 \mu, 4.5 \mathrm{M}$ | $161 \mathrm{~mm}^{2}$ | MCM-736 | $\$ 486$ |

Table 2. The manufacturing costs for other desktop RISC and $\times 86$ processors span a wide range. *multichip module; die area is for CPU chip only. (Source: MDR Cost Model)

These cost advantages apply to Pentium Pro as well. As Table 2 shows, the 0.5 -micron version now comes in at \$182, comparable to the high-end RISC chips, but the Intel processor includes 256 K of cache not found on the RISC products. The 0.35 -micron Pentium Pro, with 256 K of cache, costs just $\$ 144$. Of course, the RISC chips also benefit from a process shrink; for example, UltraSparc-2, which Sun expects to ship in 3Q96, drops to $\$ 108$ in a more advanced process.

The PowerPC chips fare well against Intel's. The 603e, which delivers integer performance comparable to a $0.5-$ micron Pentium, costs just $\$ 29$ to build, much less than Intel's cost. The 0.35 -micron Pentium reduces this gap, but cost of the 603 e will fall when it, too, moves to the 0.35 micron level in 2Q96. The $133-\mathrm{MHz} 604$ fares less well; at $\$ 80$, it is twice the cost of Pentium, although it delivers slightly better performance. Of the other RISC families, MIPS is the only one to deliver Pentium performance at a lower cost: the R5000 comes in at just $\$ 31$.

The changes in the model had a similar effect on embedded processors. Hitachi's SH7604, shipping in high volume to Sega, fell from $\$ 11$ to $\$ 8$, for example. (See 1004CW.PDF for more cost data on embedded chips.)

The model shows the best route to low cost and high performance is to move to leading-edge processes as quickly as possible while keeping die size below $100 \mathrm{~mm}^{2}$. With Intel leading the IC process race and in compacting its designs, it dominates the other x86 vendors in cost/performance while staying ahead of many of the RISC vendors as well. $\boldsymbol{D}$

MDR frequently updates its cost model to improve its accuracy. We welcome your feedback; please contact us.

